List of the Standard Cell (November 1, 2007)

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This file lists the 83 cells in the cell library distributed in the first release of the VTVT 0.18μm Standard Cell Library.

Table 1: Cells Contained in the Library vtvt_tsmc180

Cell Name	Function
buf_[1,2,4]	Noninverting buffer, drive strength 1, 2, or 4
inv_[1,2,4]	Inverter, drive strength 1, 2 or 4
and2_[1,2,4]	2-input AND gate, drive strength 1, 2, or 4
and3_[1,2,4]	3-input AND gate, drive strength 1, 2, or 4
and4_[1,2,4]	4-input AND gate, drive strength 1, 2, or 4
or2_[1,2,4]	2-input OR gate, drive strength 1, 2, or 4
or3_[1,2,4]	3-input OR gate, drive strength 1, 2, or 4
or4_[1,2,4]	4-input OR gate, drive strength 1, 2, or 4
nand2_[1,2,4]	2-input NAND gate, drive strength 1, 2, or 4
nand3_[1,2,4]	3-input NAND gate, drive strength 1, 2, or 4
nand4_[1,2,4]	4-input NAND gate, drive strength 1, 2, or 4
nor2_[1,2,4]	2-input NOR gate, drive strength 1, 2, or 4
nor3_[1,2,4]	3-input NOR gate, drive strength 1, 2, or 4
nor4_[1,2,4]	4-input NOR gate, drive strength 1, 2, or 4
xor2_[1,2]	2-input XOR gate, drive strength 1 or 2
xnor2_[1,2]	2-input XNOR gate, drive strength 1 or 2
mux2_[1,2,4]	2-to-1 multiplexer, drive strength 1, 2, or 4
mux3_2	3-to-1 multiplexer, drive strength 2
mux4_2	4-to-1 multiplexer, drive strength 2
ABnorC	(ip1*ip2+ip3)', drive strength 1
ABorC	ip1*ip2+ip3, drive strength 1
ab_or_c_or_d	ip1*ip2+ip3+ip4, drive strength 1
Not_ab_or_c_or_d	(ip1*ip2+ip3+ip4)', drive strength 1
fulladder	One-bit ripple-carry adder, drive strength 1
bufzp_2	noninverting tristate buffer, low-enabled, drive strength 2
invzp_[1,2,4]	inverting tristate buffer, low-enabled, drive strength 1, 2, or 4
cd_8	clock driver, drive strength 8
cd_12	clock driver, drive strength 12

cd_16	clock driver, drive strength 16
lp_[1,2]	high-active D latch, drive strength 1 or 2
Lrp_[1, 2, 4]	high-active D latch with asynchronous low-active reset and drive strength 1, 2, or 4
Lrsp_[1, 2, 4]	high-active D latch with asynchronous low-active reset and asynchronous high-active set, drive strength 1, 2, or 4
Dp_[1,2,4]	rising-edge triggered D flip-flop (with 1, 2, or 4 drive strength)
Drp_[1,2,4]	rising-edge triggered D flip-flop with asynchronous low-active reset (1, 2, or 4 drive strength)
drsp_[1,2,4]	rising-edge triggered D flip-flop with asynchronous low-active reset and asynchronous high-active set
dksp_1	rising-edge triggered D flip-flop with asynchronous active high set and extra inverted output.
dtsp_1	rising-edge triggered D flip-flop with asynchronous active high set input and serial scan input.
dtrsp_2	rising-edge triggered D flip-flop with asynchronous low-active reset, asynchronous high-active set, and serial scan input
jkrp_2	rising-edge triggered JK flip-flop with asynchronous active-low reset and extra inverted output, drive strength 2.
filler	filler cell (empty cell with power and ground rails and nwell)