Layout Component Placement

Author: Chenyuan Zhao

1. Open the library manager, “Tools → Library Manager”, open the schematic you wish to generate a layout of (in this tutorial we use the schematic in cell T1). Make sure that I/O pins have been placed correctly.

2. Open Layout XL from schematic menu.
3. After selecting this option, a small dialog box will first open to let users select the cell name and view name for the layout. Upon finished the selection of the cell name and view name, a Virtuoso XL layout window popup for layout generation.

4. Form the Virtuoso XL layout menu select “Connectivity → Generate → All From Source ... “. A layout generation options window appeared and then users can set pin layer (e.g. METAL 1 pin), pin width (e.g. 1), pin height (e.g. 1), boundary layer ... and so on for layout generation. Click on “Apply” after specifying the I/O pin layers to M1/pin. Make sure that “Pin Label” column is included, and choose “Label” option. Choose “Layer name” as “METAL 1” and “Layer Purpose” as “pin”, then click “OK”
After finished the selection of above information, some rectangles that represent the transistors and I/O pins will show up in the bottom of the layout window.
5. The next step is to do the device placement. The only one thing that you need to do is to place all the components and I/O pins in the layout window into the design area (cell boundary). By selecting devices/IO pins and dragging them to proper locations inside the design area, we can complete the component placement. During the device movement and placement, the lines represent the connections of select object to other objects will show up. This can help you to decide where to properly locate the selected object.

6. After you place all the components, you can use auto route to connect each device by choosing “Route → Automatic Routing...”. Make sure the configuration is the same with the following figure.
### Operate on
- Selected Set
- CellView

### Style
- Device Level

### Default Constraint Group
- virtuosoDefaultSetup

### Routing and Taper Layers
- Top Layer: METAL6
- Bottom Layer: POLY1

### Use Grid
- Manufacturing
- Routing

### Special Blockage Treatment
- Treat as Minimum Width
- Treat as Minimum Space
- Ignore Blockage Spacing
- Ignore Routespec Spacing

### Route Nets of Type
- Nets

### Miscellaneous
- Attempt to Use Double Cut Vias
- Taper Pin Width

### Autorouter Extraction
- Options

### Sequence

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Then a layout with connected paths should be appeared.

7. Usually, automatic routing is not a good method to design analog circuit layout. Manually design would be introduced in “Layout Routing” part.