Schematic Creation and Transient Simulation

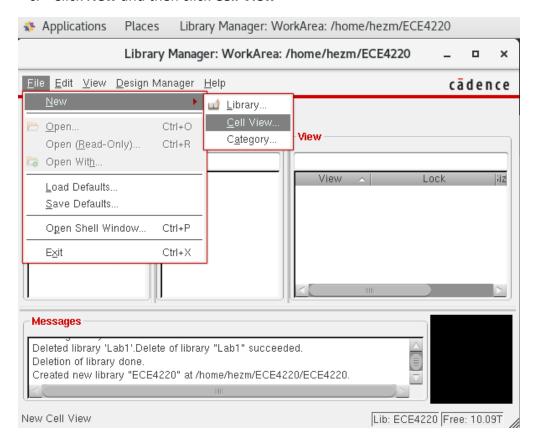
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This tutorial will guide you to build an inverter step by step.

- 1. Open Cadence Virtuoso 6.1.6 in ECE Guacamole
- 2. Open Library Manager
- 3. Create a new library (e.g.: ECE 4220)

Note: If you are not sure how to do 1, 2 and 3, please refer to "00_ Environment_Setup"

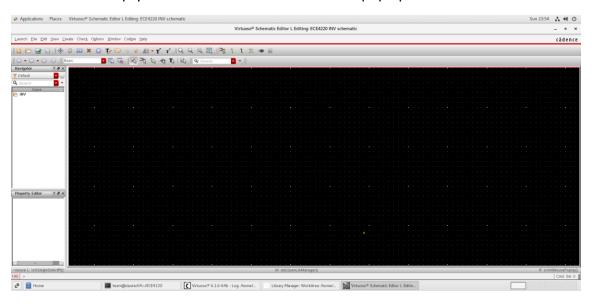
- 4. Under the library you just create, create a new cell view
 - a. Click ECE4220 under Library
 - b. Click File in the tool bar on the top of the Library Manager window
 - c. Click New and then click Cell View



- d. A New File window pops up,
 - i. For **Cell**, give a name your cell (e.g. **INV**)
 - ii. For View, set it to schematic
 - iii. For Type, set it to schematic
 - iv. For Open with, set it to Schematic L and click OK

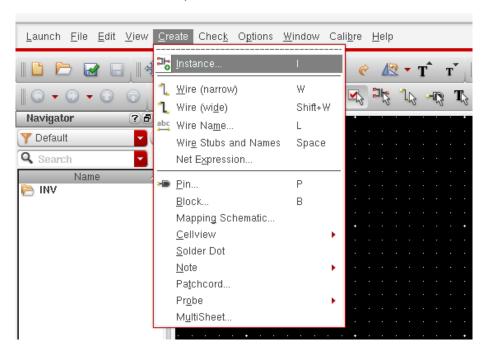


e. An empty schematic editor window should pop up

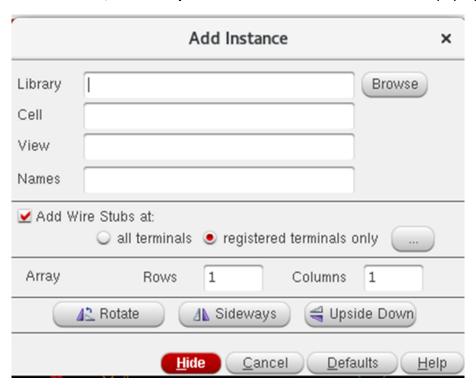


5. Place the components

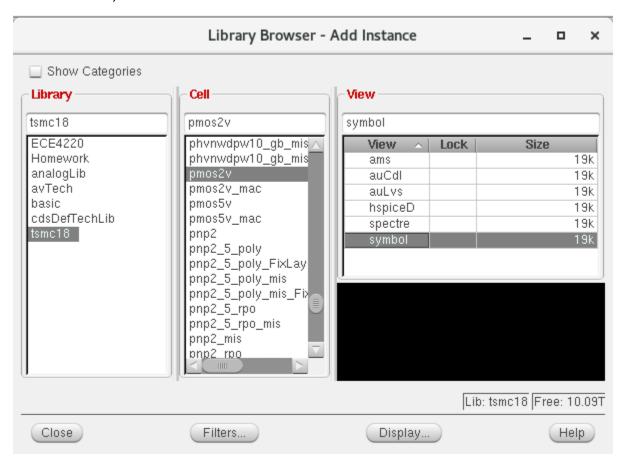
a. In the tool bar on the top of the editor, click Create, and then click Instance



b. Click Browse, the Library Browser – Add Instance windows will pop up

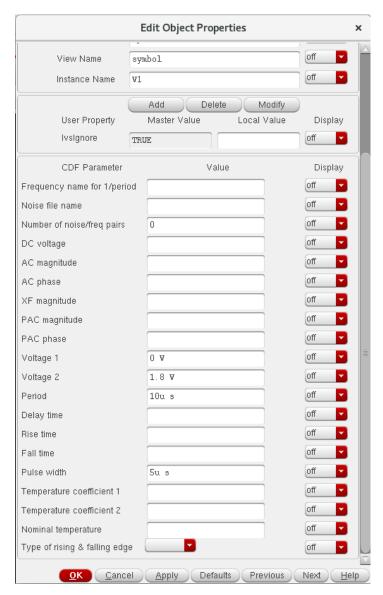


c. Click **tsmc18** under **Library**, and select **pmos2v** under **Cell**, and select **symbol** under **View**, and click **Close**



- d. Put the PMOS on the schematic
- e. Do the same for NMOS (cell name: nmos2v)
- f. Analog components such as voltage source, current source, ground can be found under the Library **analogLib**

g. For input, use "vpulse", right click on the component, click Properties, and set it up as below



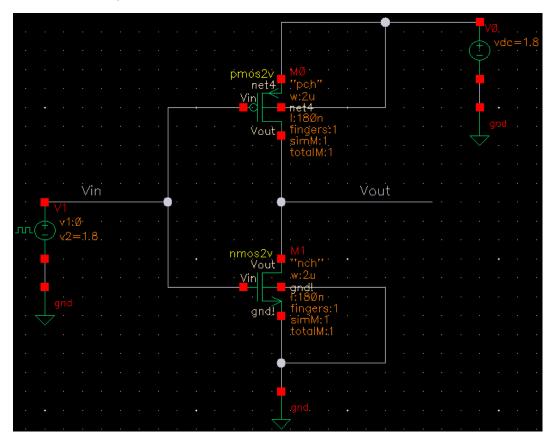
- i. For VDD, use "vdc", do the same as for "vpulse", and set DC Voltage to 1.8 V.
- h. To connect the components, select Create Narrow Wire in the tool bar



i. You may name the wires (signals) by using **Create Wire Name**, and put the tag on the wires (signals)

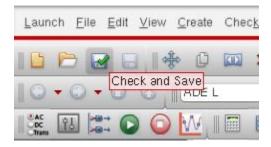


j. Below is the complete schematic for an inverter



k. Click **Check and Save** after you finish you schematic.

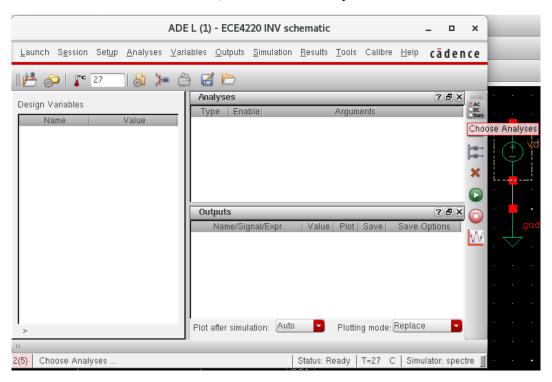
Note: Make sure you do so **every time** after you edit your schematic, otherwise errors will occur when you do simulations



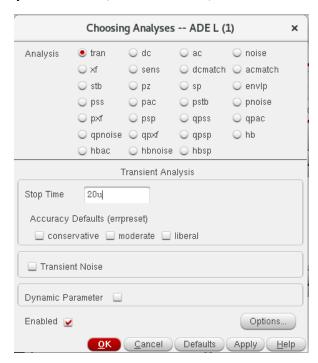
- 6. Run a transient simulation
 - a. Click Launch, and then click ADE L



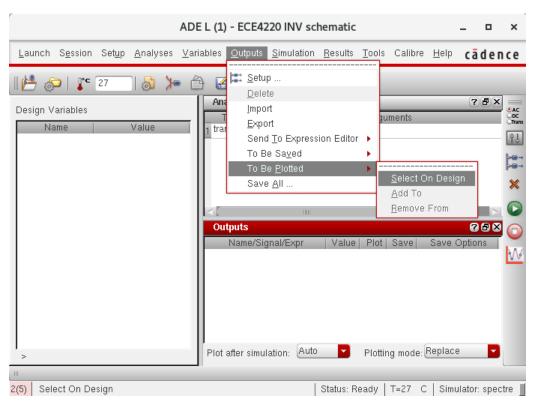
b. In the ADE L window, click Choose Analyses



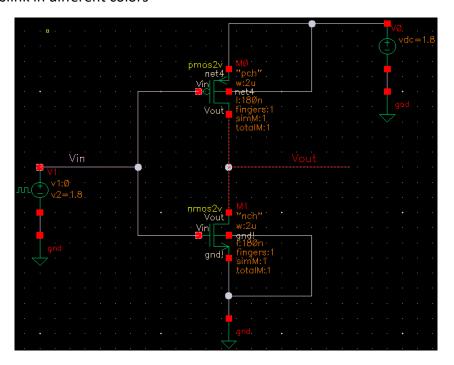
c. Set Stop Time to 20u, check Enabled, and click OK



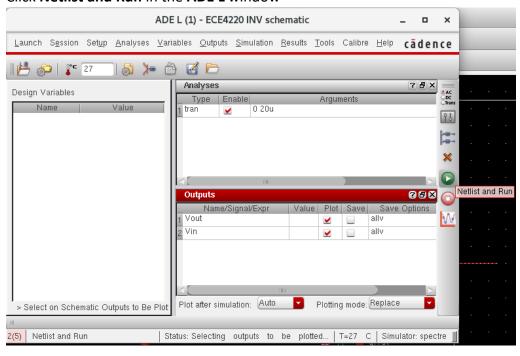
d. In the ADE L window, click Outputs, then To Be Plotted and then Select On Design



e. Click the wire (signal) where you want to plot, then the selected wires will blink in different colors



f. Click Netlist and Run in the ADE L window



g. The plot window will pop up automatically

