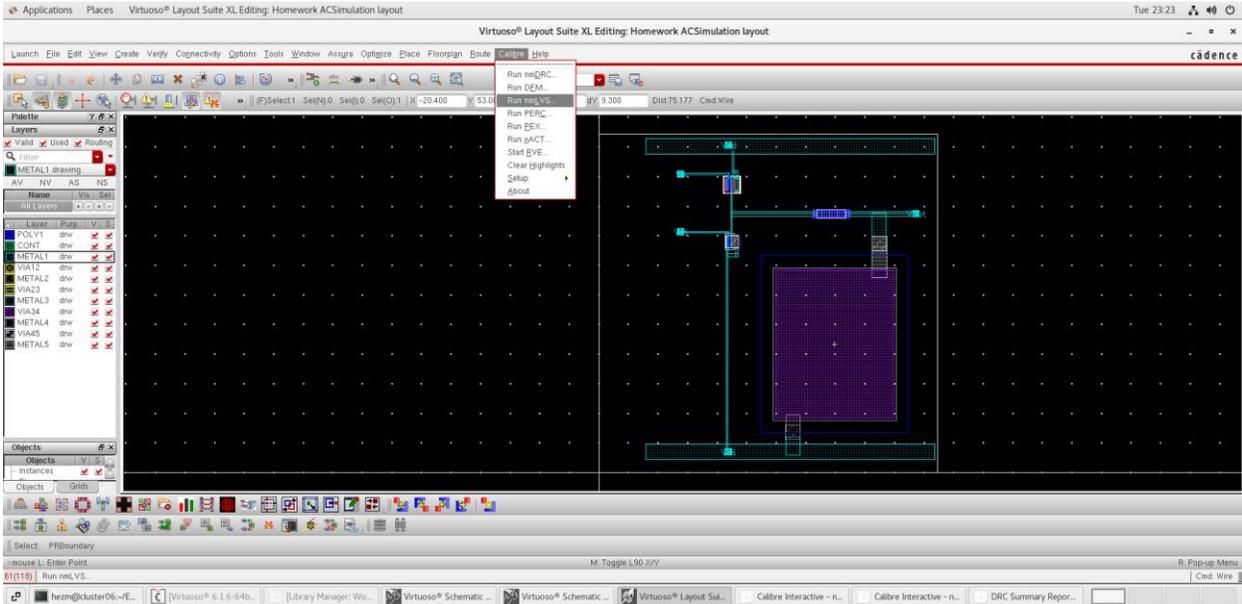


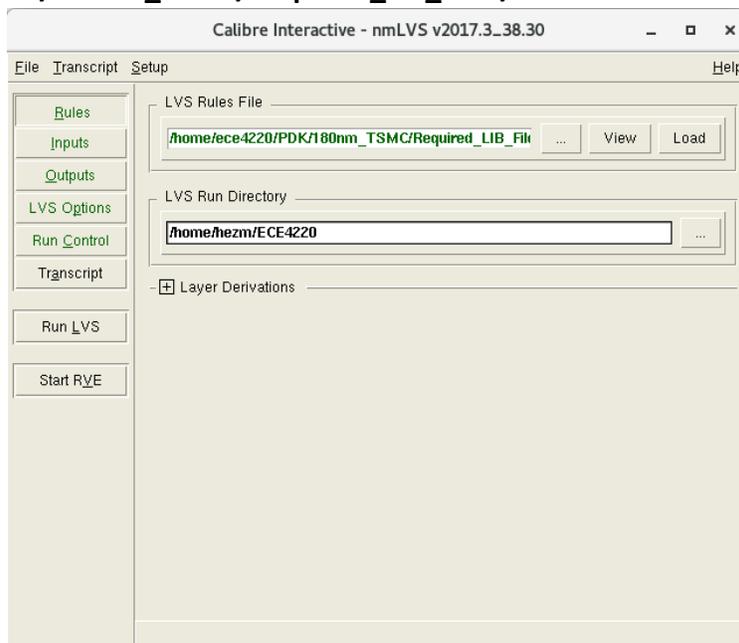
Layout Versus Schematic

Author: Jinhua Wang

1. LVS is used to check if the layout connection is correct, compared to the schematic. Click **Calibre -> Run nmLVS**.

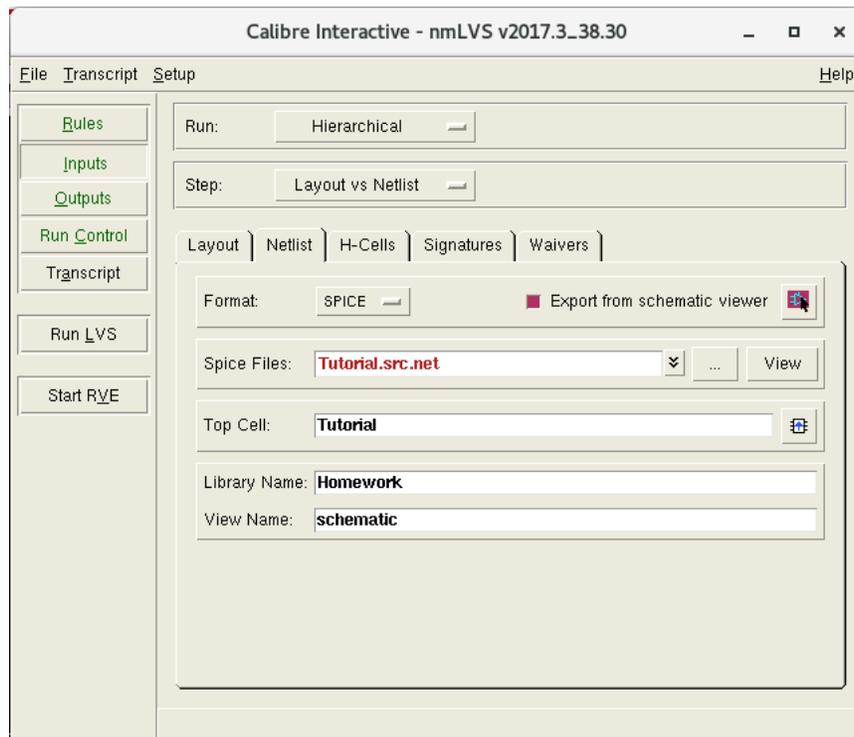


2. Click **Cancel** when the **Load Runset File** window pops up. You may save a **runset** after finishing this tutorial for later use.
3. Set the **LVS Rules File** path to **/home/ece4220/PDK/180nm_TSMC/Required_LIB_Files/calibre.lvs**



and set the **LVS Run Directory** as your **working directory**.

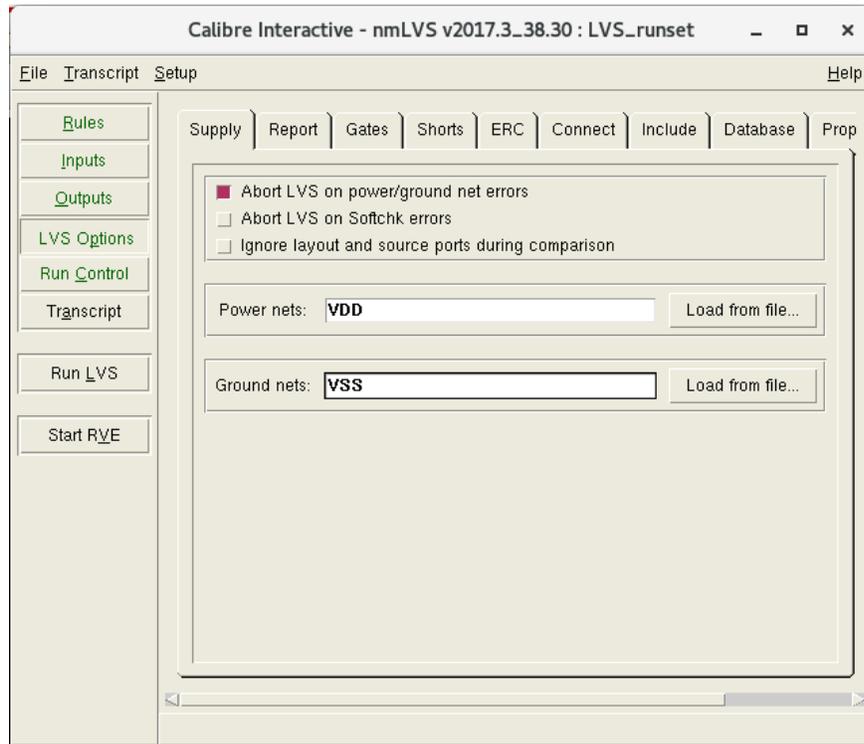
4. Go to **Inputs** -> **Netlist**, enable **Export from schematic viewer**.



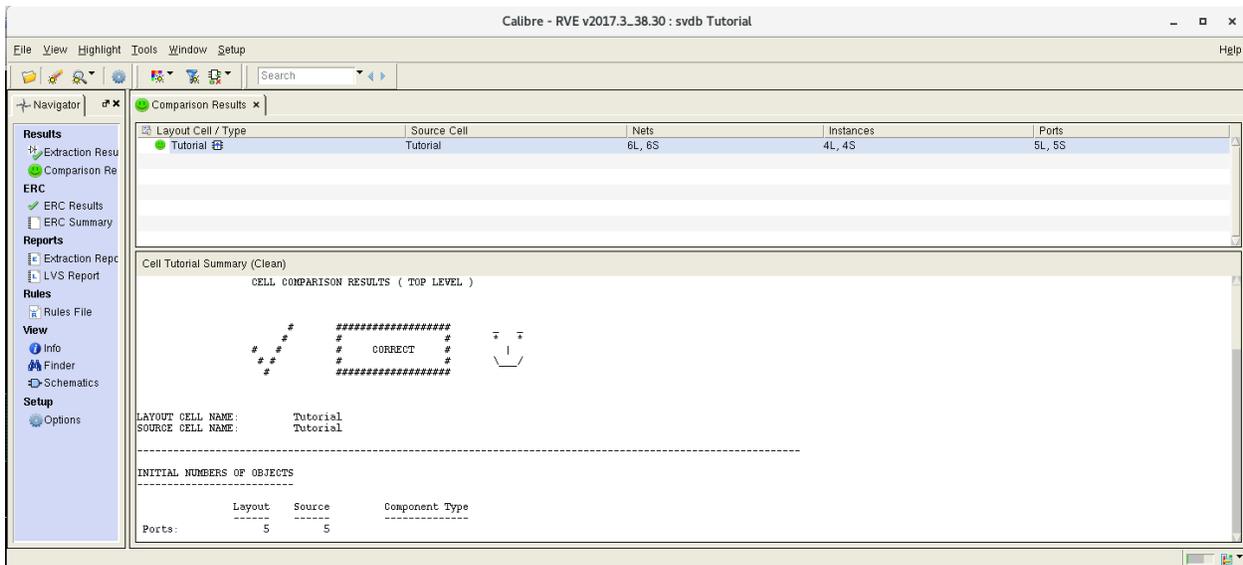
5. Go to **Setup**, enable **LVS Options**, go to **LVS Options** on the left side of the window, go to **include**, enable **Include Rule Statements**, and enter the following commands
LAYOUT CASE YES
SOURCE CASE YES
LVS COMPARE CASE NAMES



6. Go to **Supply**, for **Power nets**, enter **VDD**; for **Ground nets**, enter **VSS** (case sensitive).



7. Click **Run LVS** to run the LVS check. A report window will pop up.



Correct your layout design if any errors are reported. The report window above is **desired** (two greens checks and one smiling face).

8. You may **save** this **runset** for later use so that you do not need to set it up every time.