

# RESUME

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## PERSONAL INFORMATION

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I am now pursuing Ph.D. degree in Electrical Engineering at Virginia Polytechnic Institute and State University. My research interests lie in Analog and Mixed Mode Signal based Neuromorphic Computing design. During my Ph.D. study, I published 3 journal papers and 7 conference papers. I have been working as the group leader for two projects on design and testing the spiking analog neural encoding IC chips with Global Foundries 180 nm standard CMOS process. I also served as a technical reviewer for the International Conference on Communications (ICC), IEEE International Symposium on Quality Electronic Design (ISQED), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Multi-Scale Computing Systems (TMSCS), and etc. I have received the Robb Award in 2015 and 2016 respectively.

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## EDUCATION

- Ph.D. (cont'd), The Bradley Department of Electrical And Computer Engineering (2017 – present)  
Virginia Polytechnic Institute and State University (VT), U.S.
  - Ph.D., Dept. of Electrical Engineering and Computer Science (2014 - 2017)  
University of Kansas (KU), U.S.
  - M.S., Department of Information Science and Technology (2009 - 2012)  
JiNan University (JNU), China
  - B.S., Department of Automation (2003 - 2007)  
Nanjing University of Posts and Telecommunications (NJUPT), China
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## RESEARCH TOPICS

- Analog and Mixed Mode Signal Circuit Design
  - Neuromorphic Computing System Design
  - Reservoir Computing System design
  - Chaotic Circuit Design
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## AWARDS

- Robb Award, University of Kansas (KU) 2015, 2016.
  - Student Travel Award, ACM Student Research Competition at ICCAD, 2016
  - 3<sup>rd</sup> prize of the 12<sup>th</sup> “Challenge Cup” National Undergraduate/Graduate Curricular Academic Science and Technology (2011)
  - Outstanding Winner of the 11<sup>th</sup> “Challenge Cup” Guangdong Province Undergraduate/Graduate Curricular Academic Science and Technology (2010)
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- 1<sup>st</sup> prize Scholarship from JiNan University (2009-2011)
  - The Chinese Computer Software System Designer Certification (2006)
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## PUBLICATIONS

- [1] **C. Zhao**, Y. Yi, "When Energy Efficient Spike-Based Temporal Encoding Meets Resistive Crossbar: From Circuit Design to Application," Neuromorphic Computing Symposium: Architectures, Models, and Applications, 2017.
- [2] **C. Zhao**, J. Li, Y. Yi, "Energy efficient analog IC design for data compression in spiking neuromorphic systems," IEEE/ACM Design Automation Conference (DAC) Work-in-Progress Session, 2017.
- [3] **C. Zhao**, J. Li, and Y. Yi, "Inter-Spike Intervals (ISI) based Analog Spike-Time-Dependent Encoder for Neuromorphic Processors," IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, 2017.
- [4] **C. Zhao**, B. Wysocki, C. Thiem, N. McDonald, J. Li, L. Liu, Y. Yi, "Energy Efficient Spiking Temporal Encoder Design for Neuromorphic Computing Systems," IEEE Transactions on Multi-Scale Computing Systems, vol. pp, no. 99, 2016.
- [5] **C. Zhao**, J. Li, Y. Yi, "Analog Spiking Temporal Encoder with Interspike Intervals with Verification and Recovery Scheme for Neuromorphic Computing Systems," Accepted, IEEE International Symposium on Quality Electronic Design (ISQED), 2017.
- [6] **C. Zhao**, J. Li, and Y. Yi, "Novel Spike Based Reservoir Node Design with High Performance Spike Delay Loop," in the Proceedings of ACM International Conference on Nanoscale Computing and Communication (NANAOCOM), 2016.
- [7] **C. Zhao**, J. Li, and Y. Yi, "Making neural encoding robust and energy-efficient: an advanced analog temporal encoder for brain-inspired computing systems," in the Proceedings of IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016.
- [8] **C. Zhao**, and Y. Yi, "Novel Spiking Temporal Encoder for Brain-inspired Computing Systems" IEEE/ACM Design Automation Conference (DAC) Work-in-Progress Session, 2016.
- [9] **C. Zhao**, W. Danesh, B. T. Wysocki, and Y. Yi, "Neuromorphic encoding system design with chaos based CMOS analog neuron," Computational Intelligence for Security and Defense Applications (CISDA), 2015 IEEE Symposium, pp. 1-6, 2015.
- [10] **C. Zhao**, B. T. Wysocki, Y. Liu, C. D. Thiem, N. R. McDonald, and Y. Yi, "Spike-Time-Dependent Encoding for Neuromorphic Processors," ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 12, no. 3, pp. 23-40, 2015.
- [11] **C. Zhao**, J. Liu, F. Shen, and Y. Yi, "Low power CMOS power amplifier design for RFID and the Internet of Things," Journal on Computers & Electrical Engineering, Elsevier, 2015.
- [12] W. Danesh, **C. Zhao**, B. T. Wysocki, M. J. Medley, N. Thawdar, and Y. Yi, "Channel Estimation in Wireless OFDM Systems Using Reservoir Computing," in Proceedings of IEEE Symposium on Computational Intelligence for Security and Defense Applications (CISDA), pp. 127-131, 2015.
- [13] **C. Zhao**, Z. Zhou, Y. C. Lee, Y. Yi, "Comprehensive Ultra-broadband Design and Mode Suppression Techniques for Bends in a Differential Pair," in Proceedings of Progress In Electromagnetic Research Symposium (PIERS), pp. 1998, 2014
- [14] W. Huang, **C. Zhao**, W. Deng, J. Huang, "A New Low-Voltage CMOS Voltage Reference Design," International Conference on Electric Information and Control Engineering (ICEICE), vol. 04, pp. 74-76, 2012.
- [15] **C. Zhao**, J. Huang, "A new high performance bandgap reference," International Conference on Electronics Communications and Control (ICECC), pp. 64-66, 2011.

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## REVIEWING EXPERIENCES

IEEE Transactions on Multi-Scale Computing Systems (TMSCS)	(2016)
IEEE Transactions on Very Large Scale Integration Systems (TCAD)	(2015)
Computer & Electrical Engineering (CEE)	(2015)
Women in Computing and Informatics (WCI)	(2015)
IEEE International Conference on Communications (ICC)	(2015)
IEEE Transaction on Computer-Aided Design of Integrated Circuit and Systems (TCAD)	(2015)

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IEEE International Symposium on Quality Electronic Design (ISQED)	(2013)
International Conference on Connected Vehicles & Expo (ICCVE)	(2013)

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## PROJECT EXPERIENCES

- A spiking neuron network based Mackey-Glass (MG) nonlinear delay system has been successfully implemented by Global Foundries GFUS 7RF process. In this MG system, the delay line is constructed with analog spiking neurons. This MG chip is planning to be taped out in Feb. 7<sup>th</sup> 2017.
- Iteration scheme based temporal encoder chip design (frontend to backend). This chip contains five-neuron based iteration temporal encoder together with full bias and reference generators, signal generators, and on-chip clock generator. This chip provide another scheme to achieve temporal encoding. Asynchronous operation of each neurons makes this encoder chip more robust and accurate. Error verification scheme is also introduced in this chip to make the encoder acquiring the error resilience ability. The temporal encoding is a significant complementary technique to existing neuron chip such as TrueNorth. I finished this chip design independently with Global Foundries GFUS 7RF process (Used to be IBM 7RF process). This chip has been fabricated on Dec. 1<sup>st</sup> 2015. (09/2014 – 12/2015)
- 10MHz digital phase locking loop (PLL) system design (frontend). This PLL has minimum components including one voltage control oscillator (VCO), one charge pump, one phase frequency detector (PFD), and one ¼ frequency divider (FD). This is a course project of VLSI class. There are two people in this project and I served as team leader. (11/2015 – 12/2015)
- Chaos based random number generator design. This random number generator is based on chaotic oscillator which could provide true randomness waveform. Core nonlinear component is constructed with piecewise linear diodes. This random number generator could be served as the nonlinear controller of neural network. In other words, the technique in this random number generator provides an efficient scheme to construct dynamic neural network (09/2015-01/2016).
- Leaky Integrate and Fire (LIF) based neuron and temporal encoding chip design (frontend to backend). This chip contains independent neuron units and neuron cluster. The chip has the ability to achieve both rate encoding (with signal neuron) and temporal encoding (with neuron cluster). It is the first time to implement temporal encoding in hardware. I finished this project independently with Global Foundries GFUS 7RF process (Used to be IBM 7RF process). This chip has been fabricated on Dec. 1<sup>st</sup> 2014. (07/2014 – 12/2014)

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## TECHNIQUE SKILLS

- Cadence IC Design Environment
- Synopsys HSPICE,
- Agilent Advanced Design System (ADS)
- Altium Designer
- Matlab
- C/C++

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## WORK EXPERIENCES

Analog Circuits Design Engineer (internship) in ShenZhen BoChiXin Electronics CO. Ltd. (2010-2011)

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## GRADUATE COURSES

- Adaptive Signal Processing
  - Introduction to Digital Signal Processing
  - Introduction to VLSI
  - Microwave Engineering
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- Microelectronic Design for Circuits and Systems
  - Material and Device Electronics for Integrated Circuit
  - IC Design and Test Technology
  - Semiconductor Physics
  - Analog IC Design
  - Emerging Communications Theory and Technology
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