

A LOW-POWER VARIABLE RESOLUTION ANALOG-TO-DIGITAL CONVERTER

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ABSTRACT

A method to reduce the power dissipation of analog-to-digital converters (ADCs) in wireless digital communications systems is to detect the current channel condition and to dynamically vary the resolution of the ADC according to the given channel condition. In this paper, we present an ADC that can change its resolution dynamically and, consequently, its power dissipation. Our ADC is a switched-current, redundant signed-digit (RSD) cyclic implementation that easily incorporates variable resolution. Our ADC is implemented in a 0.35 μm CMOS technology with a single-ended 3.3 V power supply. This ADC implementation has a maximum power dissipation of 6.35 mW for a 12-bit resolution and dissipates an average of 10 percent less power when the resolution is decreased by two bits.

I. INTRODUCTION

An ADC used in wireless communications should meet the necessary requirements for the worst-case channel condition. However, the worst-case scenario rarely occurs. As a result, a high-resolution and thus high-power ADC designed for the worst case is not required for most operating conditions. A solution to reduce this wasted power is to detect the current channel condition and change the resolution of the ADC dynamically such that an ADC with an appropriate resolution is used.

In this paper, a low power, variable-resolution ADC suitable for CMOS digital processes is investigated. Variable-resolution is investigated with the goal of reducing power dissipation when the resolution of the ADC is lowered. We have implemented an ADC whose resolution is dynamically adjustable according to the given channel condition.

The organization of this paper is as follows. Section 2 reviews the ADC algorithm and its advantages for our

low-power, variable-resolution ADC. Section 3 discusses the implementation of the algorithm and its components in detail. Section 4 presents the simulation results of our proposed ADC, including accuracy, speed, and power dissipation for various resolutions. Section 5 presents conclusions.

II. BACKGROUND

A cyclic conversion algorithm was used to facilitate the implementation of a variable resolution ADC. Cyclic ADCs compute a digital output using an iterative algorithm, where one bit is computed per conversion cycle. One digital word is completed in N conversion cycles for an N-bit cyclic ADC. An approach to variable resolution for a cyclic converter is simply limiting the number of conversion cycles for a lower-resolution conversion.

Wang and Wey reported a 12-bit, 0.83 MHz, 2 mW, switched-current, redundant signed-digit (RSD) cyclic converter [2]. Opening all the switches in the architecture effectively disables the switched-current converter. Since no path exists between the power supplies, steady-state power would be small when a switched-current converter is disabled.

Furthermore, we sought to reduce the power consumption of our ADC using techniques suitable to digital processes. A common component for ADCs is a comparator that produces the digital output of the ADC. For high-accuracy ADCs, high-gain comparators that use offset-cancellation techniques are often required that comparators have large power dissipation. One approach to reduce the comparator power dissipation is to reduce or eliminate the need for high-gain components with offset-cancellation. This objective is accomplished by adopting a conversion algorithm immune to offsets. It has been shown the RSD cyclic algorithm is immune to

loop and comparator offsets, consequently reducing the comparator requirements of the ADC [1], [2].

Finally, switched-current techniques are appropriate for digital processes where precision analog components are not required. Thus, we adopted Wang and Wey's cyclic converter as the basis for implementation for our variable-resolution ADC.

III. THE ADC ARCHITECTURE and IMPLEMENTATION

A conventional cyclic ADC applies an iterative algorithm to determine the digital output of the ADC, where the input of the ADC can be a current or a voltage. Specifically, a cyclic ADC calculates one bit per conversion cycle. An ADC based on the redundant signed-digit (RSD) algorithm is a cyclic ADC with a ternary alphabet $\{-1, 0, 1\}$ rather than a binary alphabet $\{0, 1\}$. The use of a ternary alphabet for a RSD cyclic ADC makes it tolerant of loop offsets and comparator inaccuracy.

The ADC investigated in this research has variable resolution and is based on the RSD cyclic algorithm. In order to implement variable resolution, the number of conversion cycles is simply limited to n clock cycles for an n -bit digital output word, where n is dynamically set in the range of 1 to N . To save power, the current copiers can be disabled during the period when no output bits are being computed.

3.1 Architecture of the ADC

The ADC architecture that we have implemented is based on Wang and Wey's current-mode, RSD cyclic ADC architecture [3]. The ADC architecture is shown in Figure 1.

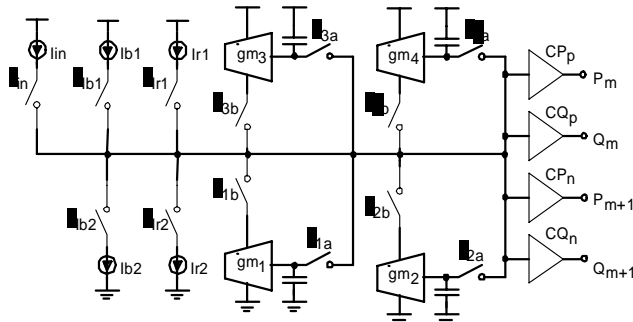


Figure 1. Analog-to-Digital Converter Architecture

The current source I_{in} is the input current of the ADC. The g_m blocks are regulated-cascode current copiers used to double the residue current. Blocks g_{m1} and g_{m2} are NMOS regulated-cascode current copiers, and blocks g_{m3} and g_{m4} are PMOS regulated-cascode current copiers. The four comparator blocks produce the digital outputs of the ADC, P_m , Q_m , P_{m+1} , and Q_{m+1} . The comparators are strobed, cross-coupled inverter comparators. The reference currents I_{r1} and I_{r2} are equally valued regulated-cascode current sources used to add and subtract the reference current as required by the RSD cyclic algorithm. The equally valued constant bias currents I_{b1} and I_{b2} are regulated-cascode current sources used to create an offset in the residue current.

3.2 Regulated-Cascode Current Copier

The regulated-cascode current copier is the major computational unit of our ADC architecture and limits the accuracy and speed of our ADC. The design considerations of the regulated-cascode current copier include the sizes of the transistors of the current copier, the operating point, and charge injection. We describe the implementation of the NMOS regulated-cascode current copiers.

The sizes of the transistors of the regulated-cascode current copier are important in the determining the speed and accuracy of the current copier. The memory transistor, its gate capacitance, and the size of the regulating transistor determine the speed of the current copier, while accuracy is largely determined by charge injection considerations. The sizes of the regulating and cascode transistors also affect the output resistance of the regulated-cascode current copier and, consequently, its accuracy. The circuit diagram of the regulated-cascode current copier is shown in Figure 2.

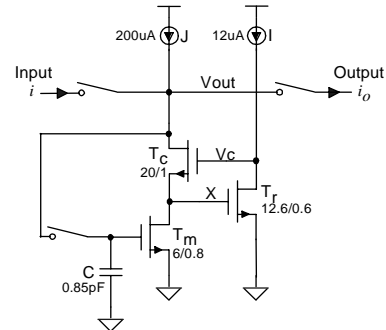


Figure 2. NMOS Regulated-Cascode Current Copier

The time constant of the regulated-cascode current copier when storing current can be shown to be the ratio of the size of the capacitor of the current copier to g_m , the small-signal input conductance of the memory transistor [4].

The time constant τ of the regulated-cascode current copier is chosen to be 1.2 ns where the gate capacitance of the memory transistor is 0.85 pF and g_m is 728 $\mu\text{A/V}$. The capacitor was implemented using double-poly layers where the unit size capacitance is 8.9×10^{-4} pF/ μm^2 . The value for g_m is obtained with $\mu_n C_{ox} = 158$ $\mu\text{A/V}^2$, $W = 6$ μm , $L = 0.8$ μm , and $V_{ds} = 0.6$ V. The size of the memory transistor and the gate capacitance of the memory transistor were fine-tuned to minimize the settling time of the current copier while maintaining accuracy. The area of the current copier is 82×137 μm^2 .

3.3 Comparators

Strobed, cross-coupled inverter comparators are used to determine the output bits of the ADC each bit cycle. These simple comparators can be used since the RSD algorithm tolerates large offsets in the comparison levels.

The strobed, cross-coupled inverter comparators of Figure 1 were implemented using small inverters. The transistors of the comparator need not be large, since the settling time of the analog components of the ADC is much greater than that of the comparators. Thus, the dynamic power dissipation of the comparators is minimized. The circuit diagram of the strobed, cross-coupled inverter comparator is given in Figure 3 with the sizes of the transistors. The area of the comparator is 26×24 μm^2 .

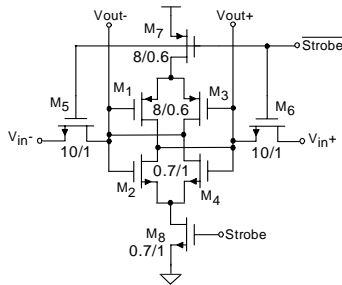


Figure 3. Strobed, Cross-Coupled Inverter Comparator

3.4 Layout

The layout of our ADC is given in Figure 4. The upper portion of the layout is the analog component of the ADC, while the lower portion is the digital portion of the ADC. The digital and analog components were separated to prohibit digital noise from propagating to the analog

component. Excluding the pad ring, the area is approximately 1.26 mm^2 .

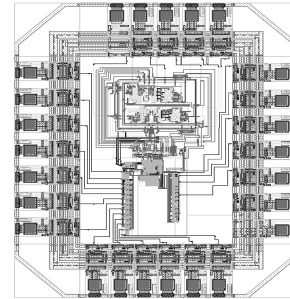


Figure 4. ADC Layout

IV. EXPERIMENTAL RESULTS

All simulation results reported in this chapter were obtained using Avant! HSPICE with a clock frequency of 1.7 MHz and a singled-ended supply voltage of 3.3 V. For all simulation results, the input bias voltage V_{bpi} is 2.3 V, and the input bias voltage V_{bi} is 0.8 V.

4.1 Power Dissipation

The power dissipation of our ADC was estimated for six different resolutions. The input current was set to 90 μA during the experiment, which gives the maximum power dissipation for the given resolution. Also, a clock frequency of 1.7 MHz and a single-ended 3.3 V supply voltage were used for the experiment. The power estimations found through HSPICE simulation are given in Figure 5. Note that the power dissipation of the input/output (I/O) pins of the chip have not been included in the power estimations presented except for the input voltage I/O pin.

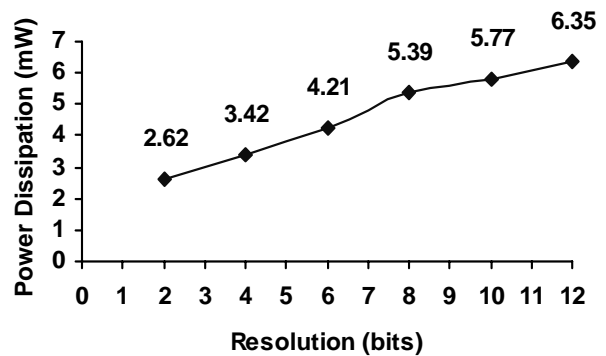


Figure 5. Maximum Power Dissipation versus Resolution

As shown in Figure 5, the maximum power dissipation for a 12-bit resolution is 6.35 mW, and the maximum power dissipation for a 2-bit resolution is 2.62 mW. The figures show that the power dissipation is approximately proportional to the resolution of the ADC. The trend is that when the resolution is decreased by two bits, the average power savings is 10 percent. Thus, our ADC is suitable for wireless communications applications where the resolution can be dynamically adjusted.

The average power dissipation of the components for a 12-bit resolution estimated over the period necessary to produce a 12-bit word is summarized in Table 1.

Table 1. Power Dissipation of the Components of the ADC

Block	Power Dissipation (mW)
Input Circuit	1.30
4 Voltage References	1.62
ADC Core	3.16
Digital Component	0.27
Total	6.35

4.2 Speed

The settling time for the ADC was found to be 300 ns. The settling time is greater than expected due to the non-ideal interaction between the regulated-cascode current sources of the architecture and the regulated-cascode current copiers. Since the clock speed of our ADC is determined by the settling time of the current copiers, the clock period of our ADC is 300 ns. As the ADC requires two clock cycles to produce one output bit, the bit rate is 1.7 MHz and the word rate is 139 kHz.

V. CONCLUSION

The ADC proposed in this paper is based on a switched-current technique. A switched-current technique is

appropriate for digital processes since precision analog components are not required. The major component in switched-current architectures is the current copier, which stores current. The current copier used in the proposed ADC is the regulated-cascode current copier. We chose to use this current copier due to its high degree of accuracy, moderate circuit complexity, and low power dissipation.

Variable resolution is implemented through digital techniques. The finite-state machine that controls the switches applies the voltages necessary to open the switches of the ADC when the desired number of bits has been computed. When the desired number of bits has been computed, the ADC is disabled and dissipates little steady-state power. Thus, the power dissipation of our ADC is reduced significantly when a lower resolution is used.

Our ADC is implemented in a 0.35 μm technology with a single-ended 3.3V power supply voltage with an active area of 1.26 mm^2 . The maximum resolution of our ADC is 12 bits with a maximum estimated power dissipation of 6.35 mW. The power dissipation decreases by an average of 10 percent when the resolution is lowered by two bits. Simulation results indicate our ADC achieves a bit rate of 1.7 MHz and has a SNR of 84 dB for input frequencies less than 8.3 kHz. Thus, our ADC is appropriate for wireless communications applications where low power dissipation is necessary.

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