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I_{DDT} Testing: An Efficient Method for Detecting Delay Faults and Open Defects*

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Abstract

Some open defects in VLSI circuits may cause delay faults, and testing of open defects and delay faults remain difficult problem. In this paper, we show that i) some open defects cause delay faults and ii) those open defects and delay faults cause variations in I_{DDT} waveforms. We propose a new I_{DDT} testing method for detection of open defects and delay faults. Our method exploits the phenomenon that an open defect generates a local maximum in the I_{DDT} waveform. We present experimental results performed on two test chips.

1. INTRODUCTION

I_{DDQ} testing monitors *quiescent* power supply current. It has been an effective method for testing short faults [1]-[4]. Since open defects often do not lead to abnormally high quiescent current, I_{DDQ} testing may be ineffective for detecting open defects. I_{DDT} testing methods, which observe instantaneous or mean values of transient power supply current, have been proposed to replace or complement I_{DDQ} testing [5]-[8]. Sachdev et al. proposed an I_{DDT} testing method, which employs a current probe to monitor transient current [7]. Min and Li proposed an I_{DDT} testing method based on measuring the mean value of transient currents [8]. They showed that their proposed method can detect open faults which cannot possibly be detected by stuck-at fault testing or I_{DDQ} testing methods. Different approaches for detecting open and short defects were studied in [9]-[11]. Germida et al. and Plusquellic et al. investigated monitoring transient voltages to detect those types of faults [9], [10]. Kim et al. suggested the use energy consumption ratio to cover such faults [11]. In this paper, we investigate the capability of I_{DDT} testing in detecting opens and delay faults.

The paper is organized as follows. Section 2 gives preliminaries necessary to understand our proposed method. Section 3 describes relationships between open defects, delay faults, and I_{DDT}. We also propose our method, which exploits the relationships. In Section 4 we present experimental results performed on two test chips. Section 5 summarizes the paper.

2. PRELIMINARIES

I_{DDT} is a transient power supply current which flows into a circuit through V_{DD} pin in the transient state of the CUT. It is the sum of transient currents of individual gates of the circuit. Transient currents of a CMOS inverter for two different slopes of the input are shown in Figure 1. The figure shows that as the slope of the input signal becomes less steep, the transient current is delayed longer, i.e., the starting point, the peak point, and the stopping points of the

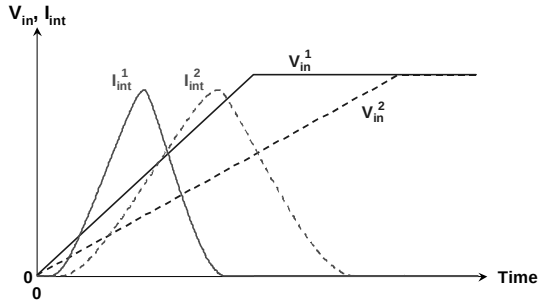

Figure 1: Transient current of a CMOS inverter.

* The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

transient current are delayed in time.

Some open defects make the defective node voltages to rise slowly, and the slow rise of a node voltage delays the waveform of the transient current. This suggests that I_{DDT} testing may be used to detect some open defects. Moreover, since delay of an input signal due to a delay fault also delays the transient current of the gate, I_{DDT} testing can possibly be used to test such delay faults. We examine the relationship between open defects, delay faults and I_{DDT} in Section 3.

Let us consider a path $P = \{g_0, g_1, g_2, \ldots, g_m\}$ of a CMOS circuit, where g_0 is the input node of the path P, and $g_1, g_2, \ldots, g_m$ are the output of the logic gate $G_1, G_2, \ldots, G_m$ on the path, respectively. Suppose that a test vector pair $T = <V_1, V_2>$ activates the path P. Let $\tau_0, \tau_1, \ldots, \tau_m$ as the signal transition timing of node $g_0, g_1, \ldots, g_m$, respectively. The overall transient current of the path is superposition of transient currents of individual gates. Since the short circuit current of gate G_i is peak at τ_i, local maximums may occur at $\tau_0, \tau_1, \ldots, \tau_m$ provided individual gate delays are reasonably large. The I_{DDT} waveform of the path under slow gate delays is shown in Figure 2, which shows m local maximums at the transition points. However, it is important to note that the number of local maximums m depends on several factors such as delay, type, and size of gates on the path. Figure 3 shows the simulation result of a cascade of four 2-input NAND gates, in which an input of each gate is tied to $V_{DD,}$ and all NAND gates are designed to be slow. The figure shows four local maximums and a ringing noise.

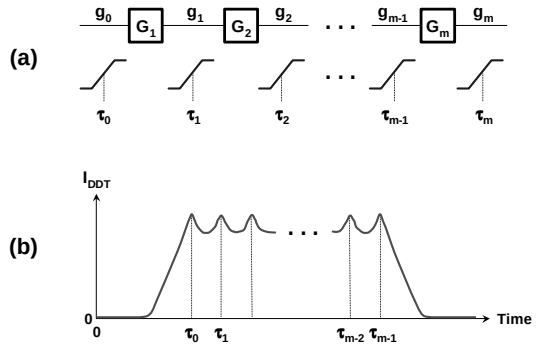

Figure 2: Transition timing and the transient current. (a) Timing diagram. (b) Transient current.

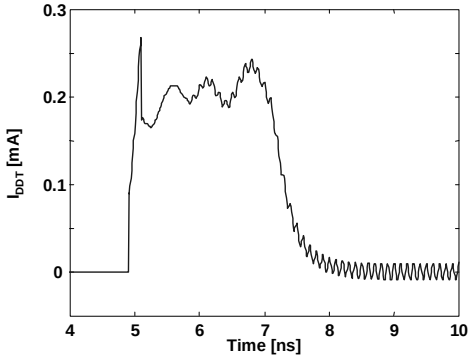

Figure 3: Transient current of a cascade of four 2-input NAND gates.

3. RELATIOSHIPS BETWEEN OPENS, DELAY FAULTS, AND I_{DDT}

We investigated relationships between open defects, delay faults, and I_{DDT} through simulation and present the results in this section. Based on the simulation results, we propose an I_{DDT} testing method, which can be used to detect some open defects and delay faults. So our method can complement existing methods for detection of open defects and delay faults. The circuit considered for the simulation is a cascade of four identical CMOS inverters as shown in Figure 4. It contains an open defect modeled as a resistor R_{open} between two nodes, IN2 and IN2*. The underlying technology of the circuit is 0.6 μm n-well process. All results presented in this section were obtained through SPICE simulation.

3.1. Opens and delay faults

First experiment is to investigate the relationship between open defects and delay faults. We varied the resistance R_{open} of the open defect from 0 Ω to 10 MΩ and measured the low-to-high (i.e., rising transition) and high-to-low (i.e., falling transition) propagation delays. The results are shown in Figure 5 (a). Delay fault size in the figure is the deference between the propagation delays of the defect-free circuit and of the defective circuits. Figure 5 shows that i) the open defect causes a delay fault for the circuit, and ii) the delay fault size is roughly proportional to the severity (equivalently resistance) of the open defect for both rising and falling transitions. The input and output voltage waveforms for four different values (0 Ω, 200 kΩ, 500 kΩ, and 1 MΩ) of open resistance R_{open} are shown in Figure 5 (b). The delay of the defect-free circuit is less than 1 ns, but the delay increases to over 10 ns for R_{open} = 1 MΩ. We tried open defects at several other locations and

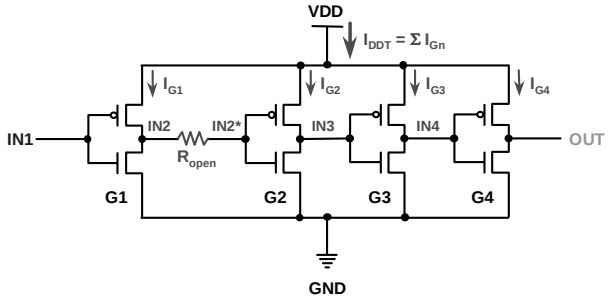

Figure 4: A CMOS inverter chain with an open defect.

noticed the same trend, i.e., the severity of the open defect increases, the delay fault size increases. Based on our observations from the experiment, *we claim that some open defects in CMOS circuits cause delay faults*.

3.2. Opens and I_{DDT}

Next, we investigated the relationship between open defects and the transient current I_{DDT}. Figure 6 shows the simulation result for four different values (0 Ω, 200 kΩ, 500 kΩ, and 1 MΩ) of the resistance R_{open}. The open defect causes the input signal of the gate G2 to rise slowly due to the increased RC delay (Refer to Figure 6 (a)). The rise time of the input signal is roughly proportional to the resistance R_{open}. The waveforms of the transient currents are shown in Figure 6 (b). As the resistance R_{open} increases, the peak of the transient current is delayed, and the duration of the current increases. Note that the peak of a transient current occurs roughly at the midpoint of the input transition. The above trend is true for open defects at some other locations. Based on the experiment, *we claim that some open defect delays the peak point of the transient current*.

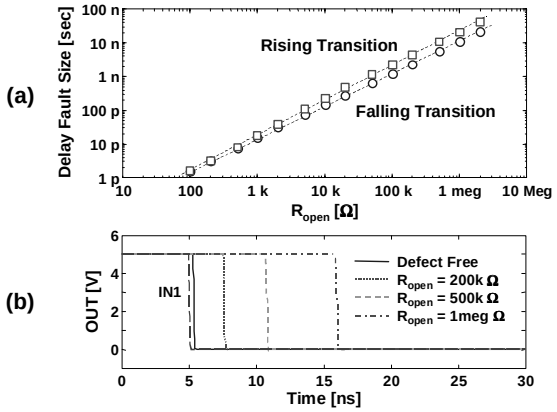

Figure 5: Delay fault size for various R_{open}. (a) Delay fault size. (b) Output waveforms.

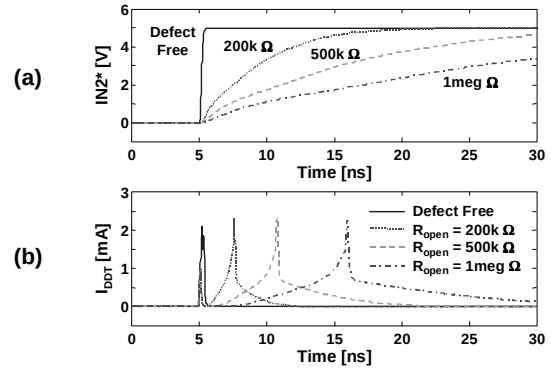

Figure 6: Transient responses of the circuit for various R_{open}. (a) Input waveforms of the loading gate G2. (b) I_{DDT} waveforms.

3.3. Proposed I_{DDT} testing method

Our simulation results show that some open defects cause delay faults and some delay faults delay the waveform of I_{DDT}. Suppose that a test vector pair $T = <V_1, V_2>$ activates a path P under test, and the test pattern V_2 is applied at time 0. Let us suppose that the output of the last gate G_m on the path switches at t_m and the delay of the gate is δ_m Then the path delay t_{pd} is equal to t_m and the input of gate G_m switches at $(t_m-\delta_m)$. If the propagation delay is $t_{pd} > T_{MAX}$, a delay fault occurred on the path. Equivalently, the path is fault free if

$$(t_m - \delta_m) < (T_{MAX} - \delta_m) \quad (1)$$

The proposed method is to observe the I_{DDT} waveform of the CUT to decide if the above condition is met or not for the test circuit. We explain our method using Figure 7. (Note that the figure is not in proportion for convenience.) *Assume that a local maximum exists at* $(t_m-\delta_m)$ *in the* I_{DDT} *waveform for a time being*. We observe the I_{DDT} waveform from time $(T_{MAX}-\delta_m)$ to a predetermined time t_f. The observation window is denoted as T_{OBSERV} in the figure. If there is one or more local maximums in the observation window, the last local maximum corresponds to the switching of gate G_m. Hence, gate G_m switches after $(T_{MAX} -\delta_m)$ to indicate occurrence of a delay fault on the path. In fact, upon detection of the first local maximum in the observation window, we can declare existence of a delay fault. It may be interesting to note that the delay fault size can be obtained from the timing of the last local maximum.

If there is no local maximum in the observation window, i.e., gate G_m switches before $(T_{MAX}-\delta_m)$, there may or may not be a delay fault. It is inclusive for our method. A

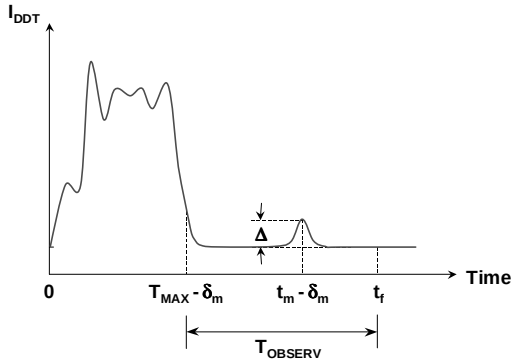

Figure 7: Proposed I_{DDT} testing method.

possible scenario is that multiple gates switch in proximity in a continuous manner between (T_{MAX}-δ_m) and (t_m-δ_m) in the observation window. When a test pattern is applied to test a path, other paths may be activated accidentally. According to our experiment performed on test chips (to be reported in Section 4), distinctive local maximums exist in the observation window under the presence of open defects (equivalently delay faults).

We discuss several practical issues regarding the proposed I_{DDT} method. First, the height of a local maximum should be above a certain threshold value (i.e. Δ in Figure 7) to immune the noise. Second, when the proposed method is used in conjunction with a delay testing method based on logic monitoring, it is a good idea to make the stopping time t_f of the observation window and the sampling time of logic values (for the delay testing method) identical. Hence, any delay fault that causes a local maximum to fall beyond the observation window will be detected by the delay testing method based on logic monitoring. Third, the gate delay δ_m varies depending on the path under test. Hence, it is necessary to set a small fixed value. Finally, an ATE system does not need to store the defect free I_{DDT} waveform, rather a threshold current in the observation current.

4. EXPERIMENTAL RESULTS OF TWO TEST CHIPS

We applied the proposed method on two test chips, an ISCAS85 benchmark circuit c6288 and a Viterbi decoder. The benchmark circuit c6288 is a combinational circuit with about 2400 gates, while the Viterbi decoder is a sequential circuit with about 2500 standard cells. CMOS transmission gates were used to introduce open defects into the test chips. Both of the circuits were synthesized, laid out, and then fabricated in the chip fabrication program of VDEC, the University of Tokyo in Japan. The technology of the test circuits is 0.6 μm n-well process.

The setup for I_{DDT} measurements is illustrated in Figure 8. The setup includes the CUT, a decoupling capacitor (C_L), a current probe (Tektronix CT-1), a digital sampling oscilloscope (Tektronix TDS754C), and an ATE system (Advantest T6671E). The ATE supplies the power and test patterns to a CUT. The oscilloscope monitors the waveform of the supply current through the current probe.

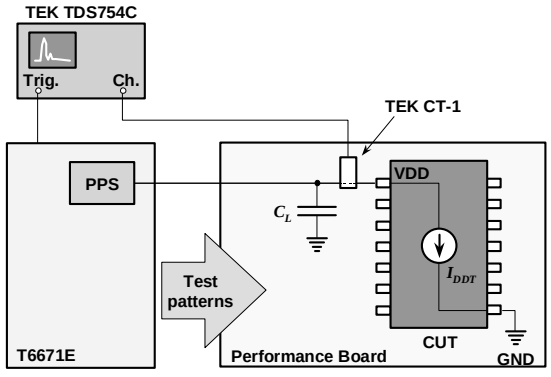

Figure 8: Setup for I_{DDT} measurements.

4.1. ISCAS85 benchmark circuit

Ten single open defects were inserted at arbitrary locations into c6288 (Refer to Figure 9.) The test circuit was measured to obtain critical path delays and I_{DDT} waveforms for two test vector pairs, T1 = < all 0, all 1> and T2 = < all 0, “00110011...0011”>.

We created a faulty circuit by introducing an open

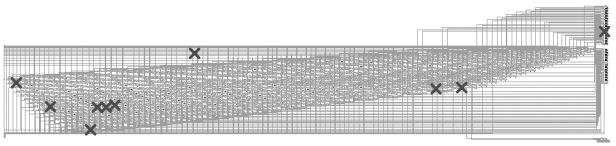

Figure 9: Locations of defects in c6288 benchmark

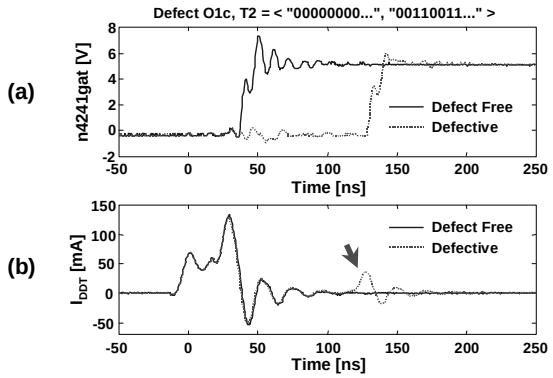

Figure 10: Experimental results for an open defect O1c. (a) Primary output signals. (b) I_{DDT} waveforms.

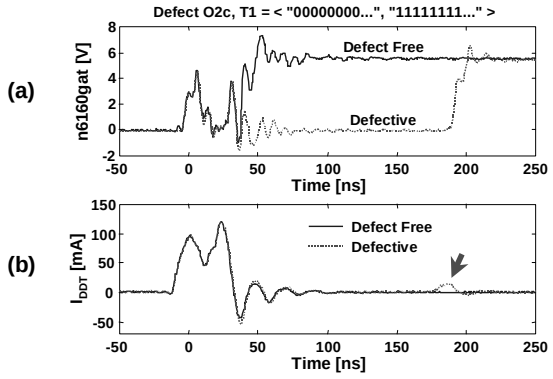

Figure 11: Experimental results for an open defect O2c. (a) Primary output signals. (b) I_{DDT} waveforms.

defect named O1c. Figure 10 shows the delay of a critical path and I_{DDT} waveforms of defect-free and defective circuits for the test pattern pair T2 in which the second test pattern was applied at 0 ns. The critical delay of the defective circuit is about 130 ns, while that of the defect-free circuit is about 45 ns (Refer to Figure 10 (a)). Therefore, the open defect causes a delay fault. On the other hand, the I_{DDT} waveform in Figure 10 (b) shows that the I_{DDT} of the defect free circuit settles down around 80 ns, while the I_{DDT} for the defective circuit has a large secondary pulse (i.e., a local maximum) starting at around 120 ns. Hence, the proposed method detects the open defect O1c provided the secondary pulse falls in the observation window. In addition, the delay fault size can be calculated, if necessary, by measuring the timing of the secondary pulse. Note that the open defect does not cause excessive I_{DDQ}, and hence an I_{DDQ} testing method would not detect the fault.

We experimented another faulty circuit with an open defect named O2c. Figure 11 shows the critical delay and I_{DDT} waveforms of defect-free and defective circuits for a test pattern pair T1, in which the second test pattern was applied at 0 ns. The open defect O2c also causes a delay fault and a variation in I_{DDT}. Like the previous case, a large secondary pulse with peak at around 190 ns appears in the I_{DDT} waveform of the defective circuit, so our method detects the fault.

Due to unavailability of a test pattern generator, we were unable to experiment the remaining eight faults. So it is inclusive if our method would detect these faults.

4.2. Viterbi decoder

We inserted two single open defects at arbitrary block into the Viterbi decoder (which is highly sequential) and measured output signals and I_{DDT} waveforms using a set of functional test vectors. Figure 12 shows the voltage waveforms of a primary output eop[1] and I_{DDT} waveforms of the defect-free circuit and a defective circuit with an open defect named O1s. The test pattern was applied at 0 ns. The output signal waveform in Figure 12 (a) shows that the primary output eop[1] of the defect-free circuit has no signal transition, while that of the defective circuit has a hazard switching back to the fault-free value "1" at around 220 ns. Like the combinational benchmark circuit, the I_{DDT} waveform of a faulty circuit has a secondary pulse at around 220 ns. So the proposed method detects the open defect. Note that the open defect causes a logic fault if it is sampled before 220 ns. So a stuck-at testing or a delay testing based logic monitoring will also detect the fault provided the value is sampled at a right time. However this fault is a redundant fault for both a stuck-at testing and a delay testing.

Experimental results with another open defect named O2s are shown in Figure 13 and 14. The open defect has no impact on all primary outputs. Output transition timings of the defect-free circuit and of the defective circuit are identical for every primary outputs (Refer to Figure 13).

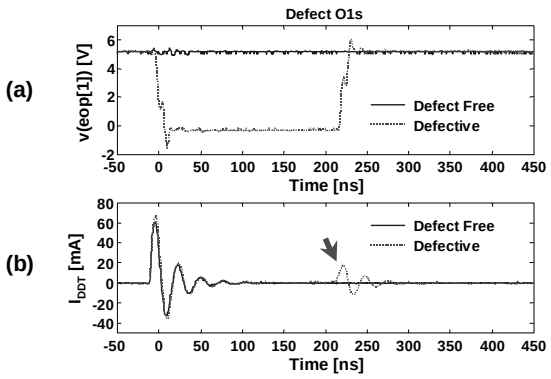

Figure 12: Experimental results for an open defect O1s. (a) Primary output signals. (b) I_{DDT} waveforms.

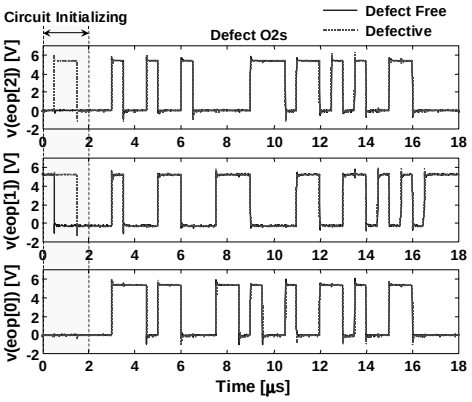

Figure 13: Primary output signals of defect-free and defective circuit for defect O2s.

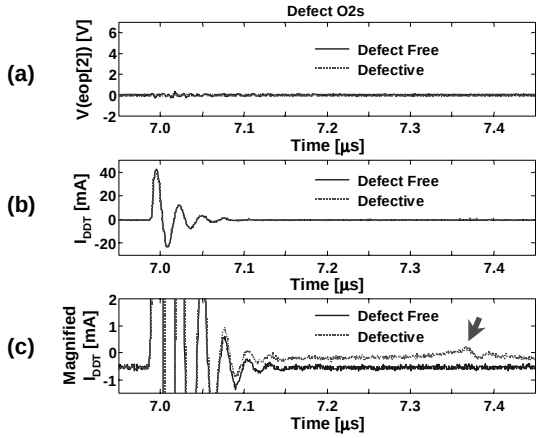

Figure 14: Experimental results for an open defect O2s. (a) Output signals. (b) I_{DDT} waveforms. (c) Magnified I_{DDT} waveforms.

This is because that the effect of the delay does not propagate to any primary output. However, the open defect causes a secondary pulse in I_{DDT} as shown in Figure 14 (c). This implies that the open defect can be detected by the proposed method but not by any testing method based on logic monitoring.

In summary, the experimental results performed on two test chips demonstrate the practicality of our method for some open defects. As we argued in the previous section, a delay fault caused by an open defect indeed generates a distinctive local maximum.

5. CONCLUSION

Shorts and opens are the major type of defects in VLSI circuits. I_{DDQ} testing has been effective for detecting short defects. Testing of open defects and delay faults remain a difficult and challenging problem. Traditional test methods based on logic monitoring are ineffective for testing open defects and/or delay faults.

In this paper, we showed, through SPICE simulations, that i) some open defects cause delay faults and ii) those open defects and delay faults cause variations in I_{DDT} waveforms. We proposed a new I_{DDT} testing method for detection of open defects and delay faults. Our method exploits the phenomenon that an open defect generates a local maximum in the I_{DDT} waveform. We demonstrated feasibility of our method through experiments performed on the two test chips. Hence, our method can be useful to complement exiting methods for detection of open defects and delay faults.

Several problems should be addressed to apply the proposed method in practice. Many factors such as process variation, drift, and the severity and location of an open defect affect the amount of abnormal current and the size of the delay defect. To make a local maximum present, a small number of paths should be activated at a time, which may necessitate logic partition. Finally, detection of local maximums for high-speed circuits may pose a technical problem.

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REFERENCES

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[1] J. M. Soden, C. F. Hawkins, R. K. Gulati and W. Mao, "I_{DDQ} Testing: A review," Journal of Electronic Testing: Theory and Applications (JETTA), Vol. 3, No. 4, pp. 291-303, 1992.

[2] S. Chakravarty and P. Thadikaran, "Simulation and Generation of I_{DDQ} Tests for Bridging Faults in Combinational Circuits," IEEE Transactions on Computers, Vol. 45, No. 10, pp. 1131-1140, 1996.

[3] R. S. Reddy, I. Pomeranz, S. M. Reddy, and S. Kajihara, "Compact Test Generation for Bridging Faults under I_{DDQ} Testing," Proceedings of VLSI Test Symposium, pp. 310-316, 1995.

[4] W. Jiang and B. Vinnakota, "Statistical Threshold Formulation For Dynamic Idd Test," Proc. of International Test Conference, pp. 57-66, 1999.

[5] S. Su and R. Makki, "Testing Random Access Memories by Monitoring Dynamic Power Supply Current," Journal of Electronic Testing: Theory and Applications (JETTA), Vol. 3, No. 4, pp. 265-278, 1992.

[6] R. Z. Makki, S. Su, and T. Nagle, "Transient Power Supply Current Testing of Digital CMOS Circuits," Proceedings of IEEE International Test Conference, pp. 892-901, 1995.

[7] M. Sachdev, P. Jamssen, and V. Zieren, "Defect Detection with Transient Current Testing and its Potential for Deep Sub-micron ICs," Proceedings of IEEE International Test Conference, pp. 204-213, 1998.

[8] Y. Min and Z. Li, "I_{DDT} Testing versus I_{DDQ} Testing," Journal of Electronic Testing: Theory and Applications (JETTA), Vol. 13, No. 1, pp. 51-56, 1998.

[9] A. Germida, Z. Yan, J. F. Plusquellic and F. Muradali, "Defect Detection using Power Supply Transient Signal Analysis," Proceedings of IEEE International Test Conference, pp. 67-76, 1999.

[10] J. Plusquellic, A. Germida, J. Hudson, E. Staroswiecki and C. Patel, "Predicting Device Performance From Pass/Fail Transient Signal Analysis Data," Proceedings of IEEE International Test Conference, pp. 1070-1079, 2000.

[11] S. Kim, S. Chakravarty and B. Vinnakota, "An Analysis of the Delay Defect Detection Capability of the ECR Test Method," Proceedings of IEEE International Test Conference, pp. 1060-1069, 2000.