IEEE Radio and Wireless Conference, pp. 367-370, September 2004, Georgia, USA

Performance Evaluation of 2D Rake Algorithms for WCDMA-DL Applications at the Handset*

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***Abstract* – Several 2D Rake algorithms have been evaluated for performance improvement over a conventional single antenna rake receiver at the handset for WCDMA downlink air interface. The main focus of the research is to study the feasibility of smart antenna algorithms for handset application and to identify the best candidate algorithm in terms of performance improvement (BLER) and relative hardware complexity (power and area requirements on a chip). The candidate algorithms are based on the following performance metrics: maximum signal-to-noise ratio (MSNR), maximum signal-to-interference-plus-noise ratio (MSINR) and minimum mean squared error (MMSE). The algorithms have been investigated for hardware complexity based on TSMC 0.18 μm technology. 3GPP specified propagation channels and test conditions have been employed to evaluate coded BLER performance. The improvement in error rate performance combined with relative hardware complexity are used to assess the feasibility of an algorithm for handset applications.**

***Index Terms* – WCDMA, 2D Rake, Handset**

I. INTRODUCTION

Smart antennas are an enabling technology that provide improved signal strength, reduced fading and thus a better link margin over a single antenna system in a communications link. Since a smart antenna system requires multiple antenna elements with more DSP processing, this technology has been mainly studied for implementation at the base station. Some examples of base station deployment are presented in [1]. Smart antenna operation within the handset form-factor has been reported in [2] for CDMA 2000 1X and CDMA 2000 1xEV-DO systems. Proposed commercial deployments of smart antenna at the handset rely on simple diversity combining technique to circumvent the increased hardware complexity issues. This approach limits the performance improvement that can be achieved with advanced beamforming algorithms. With rapid advancement in chip design, more powerful processors with lower power consumption can be available in near future that can support complex array algorithms. This paper addresses the performance of several such candidate beamforming algorithms for use at the handset for 3G WCDMA downlink applications along with the associated hardware complexity. The inclusion of smart antenna in a CDMA system gives rise to spatial as well as temporal processing (through rake processing) resulting in 2D rake receivers. This paper studies the concatenated version of the 2D Rake receiver in which resolvable multipaths are extracted from all the antenna elements and are combined first in the spatial combiners. The outputs of the spatial combiners are then fed into the temporal rake combiner. The spatial combining techniques studied in this paper are based on the following performance criteria: Maximum Signal-to-Noise Ratio (MSNR), Maximum Signal-to-Interference-plus-Noise Ratio (MSINR) or Minimum Mean Squared Error (MMSE). The temporal combiner employs Maximal Ratio Combining (MRC) scheme. Concatenated 2D Rake receivers have been previously studied for base stations (WCDMA-UL) in [3]. The handset applications of these receivers [4] were based on normalized LMS (NLMS) algorithms that usually have poor convergence behavior (compared to block processing used in some of the algorithms investigated in this paper), and were tested in Geometrically Based Single Bounce (GBSB) elliptical and circular models as opposed to 3GPP specified channels. Additionally, our paper also studies relative hardware complexity in terms of actual VHDL implementation of the algorithms using a target process of TSMC 0.18 μm with Synopsys Design Compiler and Scirocco tools. Complexity

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*This research was sponsored by Samsung Electronics Co. Ltd. in Republic of Korea

specifications include power consumption, delay and area (or gate counts). The organization of the remainder of the paper is as follows: Section II introduces system model, Section III a brief summary of the algorithms while Section IV provides the implementation details. Section V presents some selected results and Section VI draws conclusions.

II. SYSTEM MODEL

We assume a cellular communications system with a base station (single antenna) and a single mobile receiver equipped with smart antenna. Signals for different users are combined at the base station through the use of OVSF codes, and the receiver demodulates the channel-filtered desired signal in the presence of interference generated by multipaths and other users. We apply total transmit power distribution among the different users and the pilot channel based on E_c/I_{or} model. We further assume perfect power control with no handoff. The propagation channels that are used in the simulation are based on the 3GPP specified power delay profiles [5]. Fig. 1(a) and (b) show the block diagram of the transmitter and the 2D Rake receiver, respectively.

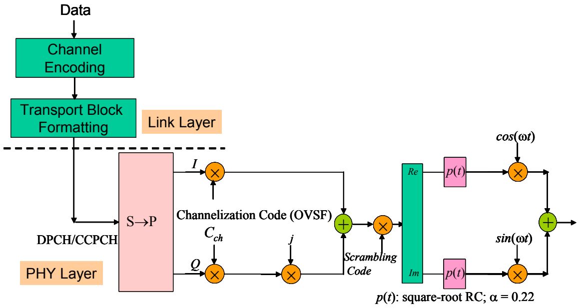

Fig. 1 (a). WCDMA-DL Transmitter

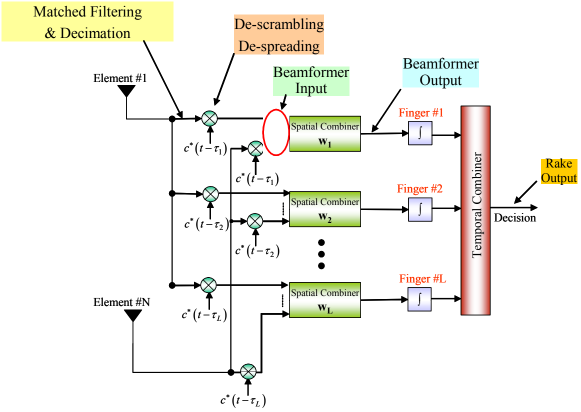

Fig. 1 (b). WCDMA-DL 2D Rake Receiver

The transmitter includes encoding and transport block formatting (Link layer functions), spreading, scrambling, modulation and pulse shaping as specified in the 3G standard. The receiver includes an *N*-element array (we limit *N* to 2 for handset applications in this paper) followed by matched filtering, descrambling and despreading to channelize all the spatial signals with the same delay to one combiner.

III. ALGORITHMS

In this section we describe briefly the different algorithms that have been tested in the spatial combining stage. The algorithms that were studied belong to the following three classes – MSNR, MSINR and MMSE. The temporal combiner uses traditional MRC to combine the beamformer outputs.

The MSNR algorithms solve a Simple Eigenvalue problem (SE) based on the covariance matrix of the desired signal and provide optimal solution when the additive noise or interference is spatially white. Maximal Ratio Combining (MRC) algorithm belonging to the MSNR class of algorithms has been used in this study, giving rise to the MRC-MRC 2D Rake structure. In the MSINR case, a Generalized Eigenvalue (GE) problem is solved based on desired signal and interference covariance matrices. For CDMA-based systems, the interference-plus-noise covariance matrix and the desired signal covariance matrix can be computed from the signal at the input and output of the despreading block, respectively [1]. There are several ways to solve the GE problem and we have studied Generalized Lagrange Multiplier method (GLM). The MMSE solution is based on the well-known Weiner-Hopf solution. The covariance matrix $\mathbf{R}_{xx}$ and the cross-correlation vector $\mathbf{r}_{xd}$ are estimated over several slots of the DPCH (containing pilot symbols). The inversion of $\mathbf{R}_{xx}$ can be done by using Direct Matrix Inversion (DMI) or through an adaptive process based on matrix inversion lemma known as the Sample Matrix Inversion (SMI) technique.

IV. IMPLEMENTATION OF THE SPATIAL COMBINERS

In this section we describe how the smart antenna algorithms were implemented for the WCDMA DL receiver. In all the algorithms we have used the downlink Dedicated Physical Channel (DPCH) to compute and update the weight vector.

A. MSNR based MRC

In the implementation of MRC, we use CPICH to obtain the channel estimates based on LS channel estimation process and use them as the weight vectors. However, we have used perfect channel knowledge and found the difference in performance (from using true estimates) to be negligible.

B. MSINR based GLM

For implementing the GLM, the interference plus noise covariance and the desired signal covariance matrices are computed based on instantaneous samples (similar to stochastic gradient approach of LMS). The received data bits are used in calculating the weight vector. Calculated weights at the end of a slot are used as initial weights for the next slot. A step size $\mu = 0.1$ is used in the weight update.

C. MMSE based DMI

The pilot symbols are exploited to estimate $\mathbf{R}_{xx}$ and $\mathbf{r}_{xd}$. The weight vector for the i^{th} slot is calculated from the received pilot symbols of the $(i-1)^{th}$, i^{th} and $(i+1)^{th}$ slots. The same weight vector is used for these three consecutive slots. The weight vector is updated after every 3 slots.

V. RESULTS

Results are provided for the following performance evaluation areas: Monte-Carlo simulations for Block error rate (BLER) performance and VHDL simulation for hardware complexity.

A. BLER Performance

The performance of the 2D rake algorithms presented in the previous section has been evaluated in simulation with WCDMA-DL air interface parameters. Some selected results are presented here and the corresponding physical channel parameters, the 3GPP specified propagation channel parameters and the test conditions used in the simulation are shown in Tables 1 (a) through 1 (c) respectively.

Table 1 (a): Parameters for simulation testing

Channel type	2 and 3 Fading
Data rate	12.2 kbps
Spreading factor SF	128
Pilot symbols	8
Number of interferers	20
CPICH Power (P_c)	0.2
Number of blocks	1500
Encoder	1/3 rate Conv.

Table 1 (b): 3GPP Propagation channels

Channel Type	Average Power (dB)	Relative Delay (ns)	Speed (km/h)
2	[0 0 0]	[0 976 20000]	3
3	[0 -3 -6 -9]	[0 260 521 781]	120

Table 1 (c): 3GPP Test Conditions

Channel Type	Geometry ($\hat{I}_{or}/I_{oc}$) (dB)	E_c/I_{or} (dB) for the DPCH	Target BLER
2	-3	-7.7	10^{-2}
3	-3	-11.8	10^{-2}

The BLER vs. E_c/I_{or} performance curves of the 2D Rake algorithms along with conventional 1D rake in fading channel type 2 and 3 are shown in Fig. 2 and Fig. 3. With the number of blocks used in the simulation (see Table 1 (a)), we have verified in a separate study that the BLER values are accurate up to 7×10^{-3}, and in this paper, we investigate the performance comparison at the target BLER of 10^{-2} as specified by 3GPP test conditions (see Table 1(c)).

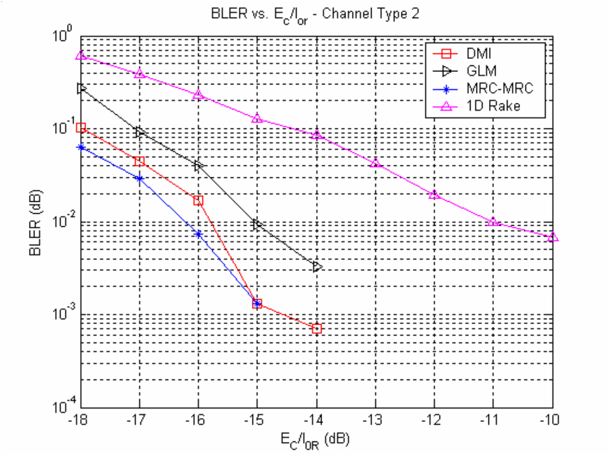

Fig. 2. BLER Performance in fading Channel Type 2

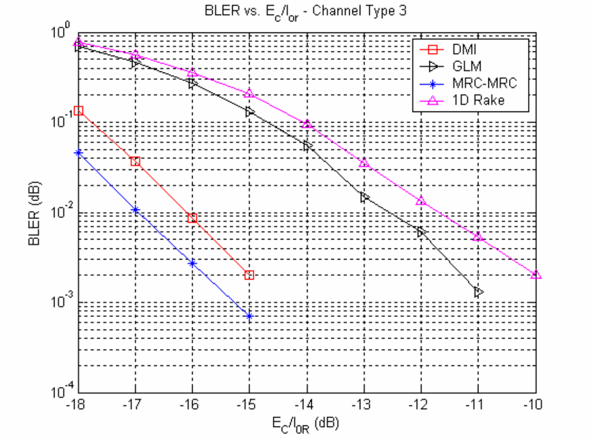

Fig. 3. BLER Performance in fading Channel Type 3

It is observed that all algorithms including 1D Rake satisfy the required test conditions (i.e., achieving target BLER within the specified E_c/I_{or}) for channel type 2, and for type 3, 1D Rake falls slightly short of the minimum requirement. From Fig. 2 we can see that the performance (at target BLER) of the MRC-MRC, the DMI and the GLM is better than that of the 1D Rake by 5.2, 4.8 and 4 dB, respectively. From Fig. 3 we see that the performance of the MRC-MRC, the DMI and the GLM is better than that of the 1D Rake by 5.26, 4.41 and 1 dB, respectively.

The findings reveal that the MRC-MRC and DMI perform the best in both the channels with the MRC-MRC having a slight gain over the DMI. The GLM performs similar to the other two except in type 3. The use of instantaneous covariance matrix instead of cumulative matrix coupled with channel PDP and mobility is considered to degrade the BLER performance of the GLM in certain channel types. The block processing nature of the DMI is seen to be robust to channel variations compared to instantaneous sample-by-sample processing of the GLM algorithm.

B. Hardware performance

We have implemented the algorithms in RTL, with VHDL from the block level specification to the pin specification. Some of the important features of the hardware implementation are shown in Table 2.

Table 2: Hardware Implementation

Operating Speed	32 kHz
Target Process	TSMC 0.18 µm
Operation Type	Signed 2's complement integer operations
CAD Tools	Synopsys Design Compiler and Scirocco

We consider the three well known but important factors for hardware implementation – power consumption, delay, and area (PDA). Power consumption is the most important issue followed by chip area in evaluating the merits of the algorithms. The comparison of the algorithms in terms of power, delay and area is shown in Figure 4. Design optimization was not attemped at this point and is left for future work.

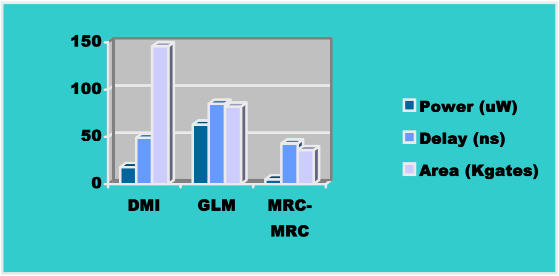

Fig. 4. Power, delay, and area comparison of 2D rake algorithms

MRC_MRC occupies the smallest area, delay, and power consumption. DMI is the second to MRC_MRC in terms of delay and power consumption except for area. Thus, we can choose the best algorithm as MRC_MRC at hardware perspectives. However, through design optimization, the DMI is expected to be competitive. The three performance metrics in hardware perspective can be traded off for resource efficient hardware implementations.

VI. CONCLUSIONS

Algorithm development and performance evaluation for 2D Rake receivers for WCDMA-DL applications have been presented in this paper. Concatenated form of 2D Rake algorithms was considered and three different beamforming criteria were studied: MSNR, MSINR and MMSE. Relative hardware complexity was also studied for the algorithms. The MRC-MRC performed the best followed closely by the DMI. This may be due to the Gaussian assumption of receiver noise and CDMA interference.

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