Design of a 4-bit 1.4 GSamples/s Low Power Folding ADC for DS-CDMA UWB Transceivers

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Abstract—**In this paper, we present a CMOS low power folding ADC (analog to digital converter) architecture, which takes advantage of the low resolution requirement of DS-CDMA UWB transceivers to reduce the power consumption. The high sampling rate is achieved by adopting current steering folding amplifiers instead of cross coupled differential pair based folding amplifiers. Our ADC adopts both resistive interpolation and multiplication to fold the input signal, thereby, reducing the number of folding amplifiers required. When this technique is applied to higher resolution converters, the power and area savings will be even more significant. A brief analysis on the operation of the folding amplifier and a systematic method for sizing preamplifiers, folding amplifiers and comparators is presented. The ADC has been designed in 0.13 μm IBM CMOS process. Post layout simulation shows that the spurious free dynamic range (SFDR) of our ADC is greater than 24 dB up to 540 MHz at 1.4 GS/s and consumes about 62 mW of power. The results also indicate that the proposed architecture consumes less power and achieves a higher sampling rate than existing folding ADCs.**

Index Terms—**DS-CDMA, SFDR, UWB, current steering folding amplifier, folding ADC, multiplier**

I. Introduction

Our DS-CDMA UWB transceiver operates for the low band from 3.1 GHz to 5.15 GHz. After the down conversion followed by a lowpass filter, the data signal occupies a bandwidth of just over 1 GHz. Our system design of the UWB transceiver requires that the ADC operate at the sampling rate of 1.3 GS/s with a 4-bit resolution. Another requirement for our ADC is a high spurious free dynamic range (SFDR) of 24 dB up to 500 MHz and low power dissipation. The low power requirement eliminates the possibility of adopting flash architectures such as the ones in [1]-[3].

A folding ADC architecture is suitable for moderate resolution and low power applications, but its sampling rate without time-interleaving is limited to a few hundred MHz so far. A time-interleaved folding ADC such as the one reported in [4] can achieve a sampling rate beyond one GS/s, but it is excluded from our consideration due to high power dissipation and high circuit complexity. Two types of folding amplifiers, one based on cross coupled differential pair (CCDP) [5] and the other based on current steering (CS) [6], have been proposed for folding ADCs. The number of comparators required for a folding ADC decreases as the folding order increases. With a CCDP folding amplifier, the parasitic capacitance at the amplifier output increases rapidly as the folding order increases, thereby, greatly reducing the achievable sampling rates [7]. In contrast, the output capacitance of a CS folding amplifier, increases much more slowly as the folding order increases [6]. However, since the transistors are stacked vertically for a CS folding amplifier, the available headroom decreases with the increase of the folding order, which makes it unsuitable for low voltage applications. So far, all existing folding ADCs employ 3X or 4X single stage folding due to this reason. Our ADC adopts 8X folding based on a CS folding amplifier to increase the sampling rate beyond GS/s. An 8X folding was achieved for our design using two 4X CS folding amplifiers along with an analog multiplier [8].

The remainder of the paper is organized as follows. Section II describes the folding ADC architecture as well as the operation of the current steering folding amplifier. Section III describes the proposed ADC design including a systematic method for optimal transistor sizing and the accompanying digital logic. Section IV presents the simulation results, and section V concludes the paper.

II. Preliminaries

This section reviews the operation of a typical folding ADC, a CS folding amplifier and an analog amplifier used for our 8X folding amplifier.

2.1 Operation of a typical Folding ADC

Fig. 1 shows a block diagram of a conventional 4X folding ADC architecture. The flash ADC produces the two MSBs splitting the search space into four regions. The 4X folding amplifiers split each of the four regions into four subdivisions and the digital encoder generates the corresponding two LSBs. Thus apart from two MSBs which require 3 comparators, the folding part requires 4 comparators.

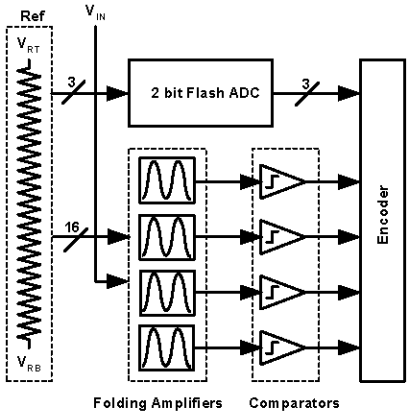

Fig. 1: Block diagram of a conventional 4-bit folding ADC

The folding architecture is a low power alternative to the flash architecture because it reduces the number of comparators required. However, the folding architecture has been limited

mostly for low resolution ADCs such as 4- to 8-bit ADCs due to technical difficulties in implementing high order folding amplifiers with high speed and/or large input bandwidth. The folding operation effectively increases the output frequency of a folding amplifier as given in the following relationship [5]. The instantaneous output frequency f_{out} is

$$f_{out} = \sqrt{2}.F_F.f_{in} \quad (1)$$

where F_F is the folding factor and f_{in}, is the input frequency. Hence, the output frequency is proportional to the folding factor, thereby, restricting the input bandwidth of the converter.

2.2 Current Steering Folding Amplifier

A key component for folding ADCs is folding amplifiers. CCDP folding amplifiers have been widely used [4], [5], [10]. A CCDP folding amplifier achieves the folding characteristic by alternately summing the positive and negative outputs of consecutive differential pairs. A CCDP folding amplifier requires as many well-matched differential pairs as the folding order. Further, a CCDP folding amplifier restricts the difference of two consecutive reference voltages ΔV_r as given below [5].

$$\Delta V_r \geq 2.\sqrt{\frac{2.I_{tail}}{\mu c_{ox}.W/L}} \quad (2)$$

where I_{tail} is the tail current of each differential pair, μ is the channel mobility, and c_{ox} is the gate oxide capacitance per unit area. This restriction is due to the fact that the zero crossings have to be sufficiently far apart to ensure that there is no overlap in the folding characteristics.

Guo et al. proposed a CS folding amplifier to address the above shortcomings [6]. A CS folding amplifier shown in Fig. 2 has several advantages over CCDP folding amplifiers. It requires only a single current source, so there is no need for matching while reducing power consumption. It has less load capacitance at the output node compared to a CCDP folding amplifier and hence has a lower settling time.

Guo et al. also claimed that their CS folding amplifier is not subject to the restriction on the difference of two consecutive reference voltages specified in (2). However, consider that the applied input voltage is in the vicinity of $V_{REF3}=0.75V_{in(max)}$. For proper operation of the 4X folding amplifier, transistors M_{A1}, M_{A2}, M_{B4} and M_{C4} must be turned on and M_{A4}, M_{B1}, M_{B2}, and M_{C2} must be turned off. Since M_{B2} is off, M_{C3} is also turned off due to the lack of a conducting path. The whole folding amplifier can now be visualized as a single differential pair. The input transistors of the differential pair are M_{A3} and M_{B3} and M_{A1} and M_{A2} provide a path to the current source. To ensure that M_{B1} and M_{B2} are turned off, the "differential pair" constituted by M_{A1} and M_{B1} and the "differential pair" constituted by M_{A2} and M_{B2} have to be saturated. Similarly, for M_{A4} to be turned off the "differential pair" constituted by M_{A4} and M_{B4} must be saturated. Therefore, we conclude that the folding amplifier proposed by Guo et al. also has to meet the restriction in (2).

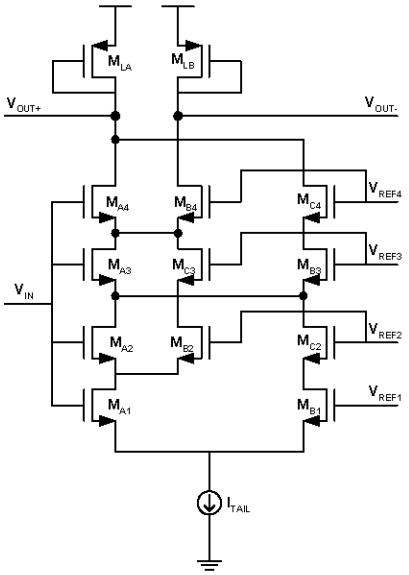

Fig. 2: Current steering folding amplifier

Among the two types of folding amplifiers, CS folding amplifiers are more favorable for a higher sampling rate and a larger input bandwidth due to low capacitance at the output node. A major problem for CS folding amplifiers is a reduced output swing voltage at a lower supply voltage, because the transistors are stacked on top of each other. The problem is even more acute, if we desire a higher order folding.

2.3 Four Quadrant Analog/RF Multiplier

A key block for our ADC is an 8X folding amplifier, which is based on a four quadrant analog multiplier presented in [8]. The analog multiplier is shown in Fig. 3. The output of the multiplier is represented by

$$V_{out} = -R_{01}R_1K_{n1}K_{n4}(V_{IN1+} - V_{IN1-})(V_{IN2+} - V_{IN2-}) \quad (3)$$

where K_{n1} and K_{n4} are the transconductance parameters $\mu C_{ox}W/L$, of transistors M_1 and M_4.The gain of the multiplier should be adjusted properly to obtain a sufficient voltage swing for an 8X folding amplifier.

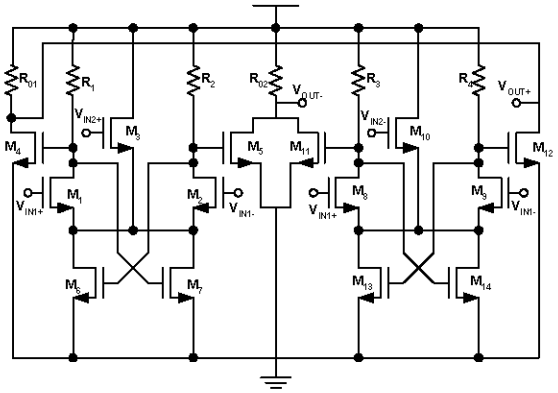

Fig. 3: Four quadrant analog multiplier

III. PROPOSED ADC DESIGN

This section describes the overall architecture of the proposed folding ADC, a technique to design an 8X CS folding amplifier, and a systematic transistor sizing scheme for three major building blocks of our folding ADC.

3.1 Overall Architecture

The block diagram of our folding ADC is shown in Fig. 4. A flash ADC generates the 2 MSBs, and the remaining two LSBs are generated from folding amplifiers. The input and the reference voltages are differential to reduce the common mode noise.

The 2-bit flash ADC consists of three preamplifiers followed by sample-and-hold (S/H) circuits. Each S/H has a dummy switch, which is always closed, to absorb charge injection effects [11]. A S/H is followed by a resistive averaging block to reduce random mismatches and offset errors [9]. The resistive averaging block distributes the mismatch currents due to process variations and smoothes out large variations.

The folding part has an array of *eight* preamplifiers followed by S/Hs. The outputs of the S/Hs are averaged by resistive averaging and then applied to *two* CS 4X folding amplifiers. The outputs of the 4X folding amplifiers are interpolated using two resistors, and the following comparator decides the third bit. The final bit, the LSB, is decided by an 8X folding amplifier, which is implemented through multiplication of the two 4X folding amplifier outputs.

The zero-crossing points of the folding amplifiers are critical for any folding ADCs. The zero-crossing points for the top 4X folding amplifier are $\frac{V_{in(p-p)}}{16}$ (1, 5, 9, 13), and that for the bottom amplifier are $\frac{V_{in(p-p)}}{16}$ (3, 7, 11, 15). When the two amplifier outputs are interpolated, the zero-crossing points become $\frac{V_{in(p-p)}}{16}$ (2, 6, 10, 14). So the comparator output can be used to determine the third bit of our ADC.

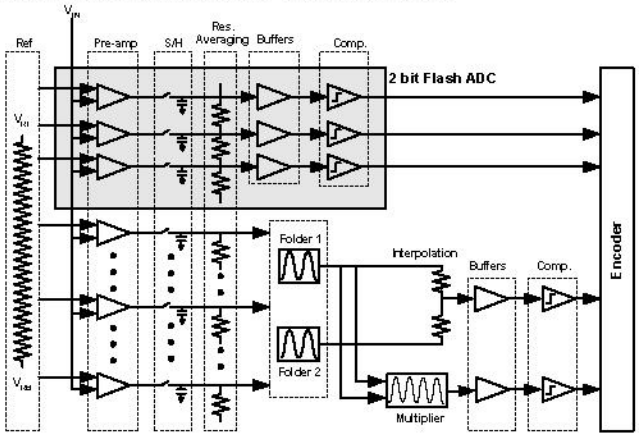

Fig. 4: Block diagram of the proposed folding ADC

As discussed earlier, a CS folding amplifier stacks transistors vertically. Hence, a direct extension of a 4X folding shown in Fig. 2 will not work for an 8X folding amplifier operating at a low supply voltage. Instead, we implement an 8X folding amplifier by multiplying the outputs of the two 4X folding amplifiers using a four quadrant analog multiplier shown in Fig. 3. The zero-crossing points of the 8X folding amplifier is the union of zero-crossing points of the two 4X folding amplifiers, and they are $\frac{V_{in(p-p)}}{16}$ (1, 3, 5, 7, 9, 11, 13, 15). The odd numbered zero crossing-points are used to determine the LSB of the ADC.

Fig. 5 shows the SPICE simulation of the two folding amplifiers, the resistive interpolation, and the multiplier output and the waveforms verify the zero-crossing points discussed above.

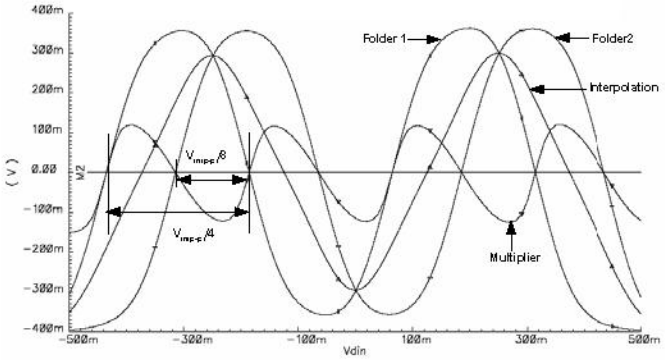

Fig. 5: Transfer characteristics of 4X and 8X folding amplifiers

Compared with the conventional ADC shown in Fig. 1, the main advantages of the proposed folding ADC architecture are low hardware complexity and high speed. The proposed ADC saves two 4X folding amplifiers and two comparators at the cost of one additional analog multiplier. So the proposed architecture reduces the overall circuit complexity to result in low power dissipation. In other words, use of only two 4X folding amplifiers to decide the two LSBs is unique for the proposed design and effective for reduction of hardware complexity and power dissipation. This technique may be applicable for higher resolution ADCs as well.

3.2 Analog Building Blocks

Like any analog circuit design, transistor sizing is a key design issue for the proposed folding ADC. Transistor sizing has been discussed in detail for flash ADCs, but little work has been done for folding ADCs [1], [2], [14]. In this section, we describe our approach to determine transistor sizes for three major building blocks: preamplifiers, folding amplifiers, and comparators. We decided initial transistor sizes based on an approximate input/output relationship of each block and then fine tuned the sizes through simulation.

The target Integral nonlinearity (INL) of our ADC is set to 0.1 LSB or $\frac{0.1V_{in(p-p)}}{16}$. So an input voltage which differs from any particular reference voltage level by at least $\frac{0.1V_{in(p-p)}}{16}$ should be resolved into the corresponding digital output code within one period of the sampling clock.

3.2.1 Preamplifier

The preamplifier considered in our ADC is shown in Fig. 6. Since the difference between input and reference voltages need to be amplified in a balanced manner, all the transistors M_1 through M_4 have the same size. A preamplifier can be considered as a single step/open loop comparator, because the comparison operation is basically voltage amplification [14]. For a single step comparator, the output voltage y_{pa} can be expressed as

$$y_{pa}(t) = d_{pa}\frac{t}{\tau_{pa}} \tag{4}$$

where d_{pa} is the input to the preamplifier and τ_{pa} is the preamplifier unitary time constant [14]. The unitary time constant τ_{pa} is expressed as C_o/g_m, where C_o is the output node capacitance and g_m is the transconductance of each input transistor. Thus, the time constant could be related to transistor sizes using the following two expressions, (5) and (6)

$$C_o = WEC_j + 2(W+E)C_{jsw} \tag{5}$$

where W is the width of the transistor, E is the width of the source/drain junction, C_i is the junction capacitance per unit area and C_{jsw} is the junction side wall capacitance per unit area. The values of E, C_j, and C_{jsw} values are specific to the process technology and were available from our design kit.

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_{tail}} \tag{6}$$

where μ_n is the channel mobility, C_{ox} is the gate oxide capacitance per unit area, W and L refer to the dimensions of the transistors and I_{tail} is the bias current of the differential pair.

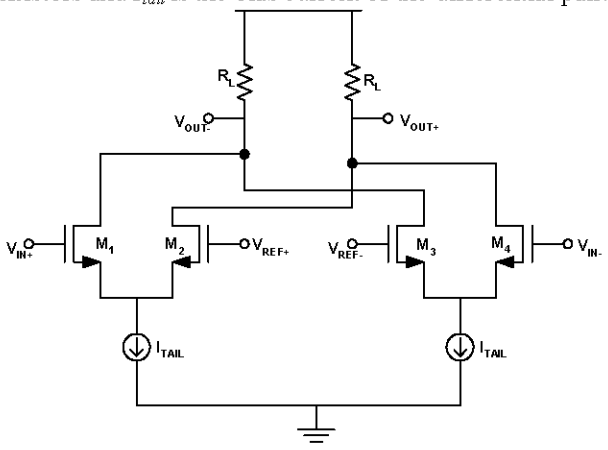

Fig. 6: Preamplifier

The linear range V_{linear} of a 4X folding amplifier can be obtained as in (7) and should be less than $V_{in(p-p)}/4$ to avoid an overlap in the folding characteristics [5].

$$V_{linear} = 2.\sqrt{\frac{2I_{tail}}{\mu_n c_{ox}\,W/L}} \le \frac{V_{in(p-p)}}{4} \tag{7}$$

For a preamplifier whose input reference voltage is away from the input voltage by more than 0.5 LSB, the preamplifier output voltage should be large enough to drive the differential pair of the following CS folding amplifier to saturation, so that the folding amplifier works as a single differential pair, as described in Section 2.2. In order to meet the required sampling rate, we set the output voltage of the preamplifier to exceed the linear input range of the following folding amplifier within 80 % of the off-phase of the clock, $T_{off,clk}$. Using the condition in (4), we obtain the following relationship expressed in (8)

$$y_{pa}(0.8T_{off,clk}) = \frac{0.5V_{in(p-p)}}{16}\frac{0.8T_{off,clk}}{\tau_{pa}} \ge V_{linear} \tag{8}$$

Using (7) and (8), we obtained the value of τ_{pa}, and then initial device sizes of M_1 through M_4 using (5) and (6).

3.2.2 CS Folding Amplifier

The sizing of the folding amplifier is also based on the expression for the preamplifier shown in (4), as a CS folding amplifier basically works as a simple differential amplifier. All the transistors in the folding amplifier have the same size to provide the same folding characteristics over the entire input range.

The minimum input voltage d_{fa} of a folding amplifier such that its output can be successfully resolved by the following comparator is the limiting case. The output voltage of a preamplifier whose input voltage is 0.1 LSB (which is the target INL) away from its reference level is the minimum input voltage d_{fa} and can be obtained as

$$y_{pa}(T_{off,clk}) = \frac{0.1V_{in(p-p)}}{16}\frac{T_{off,clk}}{\tau_{pa}} = d_{fa} \tag{9}$$

using (4). Since the folding amplifier can be viewed as a simple differential amplifier, (4) can be applied again to express the folding amplifier output $y_{fa}(t)$ as

$$y_{fa}(t) = d_{fa}\frac{t}{\tau_{fa}} \tag{10}$$

where τ_{fa} is the folding amplifier unitary time constant. To determine transistor sizes of folding amplifiers, we need to obtain τ_{fa}, and the procedure is explained below.

We set 15 % of the on-phase of the clock $T_{on,clk}$ as the settling time for the folding amplifier. Using (10), we obtain

$$y_{fa}(t) = d_{fa}\frac{0.15T_{on,clk}}{\tau_{fa}} = d_{rgc} \tag{11}$$

where d_{rgc} represents the *minimum* input voltage to the following comparator. So the remaining issue is to find d_{rgc} of the comparator and this is explained in the next section.

3.2.3 Comparator

The regenerative comparator used in our ADC is shown in Fig. 7 [2]. The output voltage of a regenerative comparator increases exponentially with time, due to positive feedback and is given as

$$y_{rgc}(t) = d_{rgc}e^{t/\tau_{rgc}} \tag{12}$$

where τ_{rgc} is the unitary time constant of a comparator [14]. During the off-phase of the clock, $T_{off,clk}$, the comparator output is shorted and stays in the quiescent state. During the on-phase, the comparator output has to reach digital level from the quiescent state within a fraction of the on-phase of the clock, $T_{on,clk}$. We set the quiescent voltage level at halfway to the supply voltage. We also set the settling time of the comparator within 10 % of $T_{on,clk}$. Therefore, the comparator output has to increase by 0.5 Vdd in $0.1T_{on,clk}$. We obtain the following using (12).

$$0.5V_{dd} = d_{rgc}e^{0.1T_{on,clk}/\tau_{rgc}} \quad (13)$$

We picked several candidate unitary time constants τ_{rgc} and then determined d_{rgc} using (13). The unitary time constants can be related to transistor sizes as follows

$$\tau_{rgc} = C_o\left(\frac{1}{g_{m,p}} \| \frac{1}{g_{m,n}}\right) \quad (14)$$

where $g_{m,p}$ and $g_{m,n}$ are the transconductance of PMOS and NMOS transistors, respectively. The output node capacitance C_o is expressed as

$$C_o = C_{DB,p} + C_{DB,n} + C_{GS,p} + C_{GS,n} \quad (15)$$

The expression for drain-bulk capacitance is given in (5), and the gate-source capacitance is approximately expressed as $C_{GS} = \frac{2}{3}WLC_{ox}$.

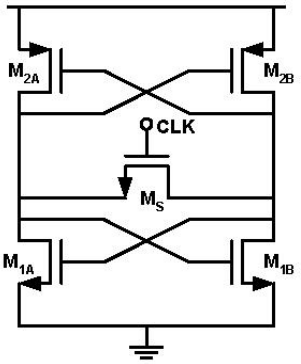

Fig. 7: Regenerative comparator

Although the above guidelines are based on approximate analyses, they proved to be an effective tool for determining initial transistor sizes and to estimate the maximum achievable sampling rate.

3.3 Digital Encoder

The block diagram of the digital encoder is shown in Fig. 8. True single phase clock (TSPC) latches capture the comparator outputs, and sense amplifier based flip-flops synchronize the inputs to the encoding logic [12], [13]. The encoding logic converts the gray-coded comparator outputs to the binary code, and another set of sense amplifier based flip-flops synchronize the encoded outputs.

In order to test our standalone ADC, we have added a decimator, which decimates the outputs by 16. An external control input selects between decimated or undecimated data at the outputs.

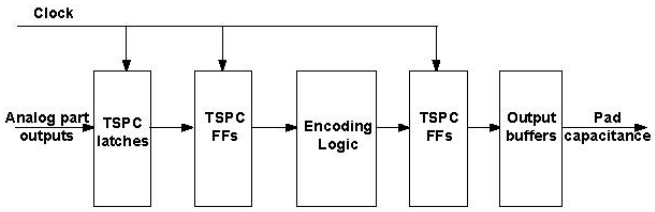

Fig. 8: Block diagram of the digital encoder

IV. POST LAYOUT SIMULATION RESULTS

The proposed folding ADC was laid out in 0.13 µm IBM CMOS technology. The layout of the core part is shown in Fig. 9. Guard rings are used around the digital circuitry to minimize cross-talk between analog and digital sections. The ADC occupied an active area of 0.05 mm^2 and consumed 62 mW at the sampling rate of 1.4 GS/s with the supply voltage of 1.5 V.

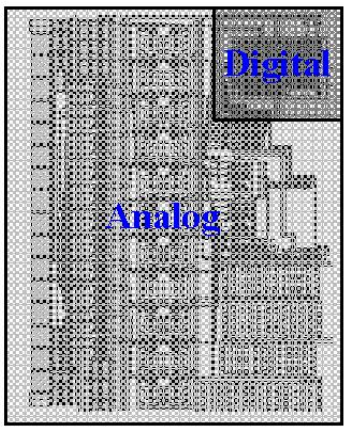

Fig. 9: Layout of the core part of the ADC

The design kit enabled use of Monte Carlo analysis as well as corner simulations. Therefore, process variations and geometric mismatches could be included in our simulation without going through a behavior model of the ADC. The maximum INL and DNL were determined with the corner parameters set to the maximum 3-sigma variation.

Fig. 10 shows INL (integral nonlinearity) and DNL (differential nonlinearity) for the entire range of the output code. The results indicate that the peak INL is less than 0.2 LSB and the peak DNL is less than 0.3 LSB. The performance is typical for a low resolution ADC and sufficient for our application. Digital calibration schemes can be used to improve the static performance at the cost of increased circuit complexity and power consumption.

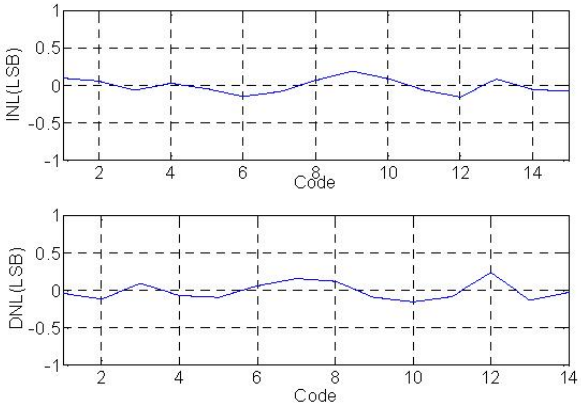

Fig. 10: INL and DNL performance

The next simulation was to estimate the variation of SFDR with an input frequency at the sampling rate of 1.4GSamples/s. The simulation results given in Fig. 11 indicate that the SFDR remains above 24 dB for up to 540 MHz.

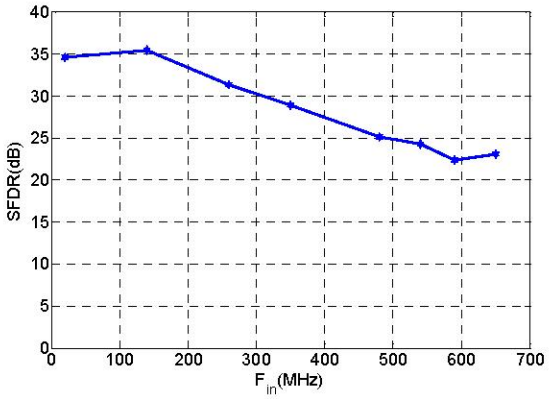

Fig. 11 SFDR vs. input frequency at F_s = 1400 MS/s

Finally, Fig.12 shows the normalized output spectrum for a single input tone of 540 MHz when the ADC is sampled at 1.4 GSamples/s. The highest spurious tone is at about 380 MHz with a power level of -24 dB.

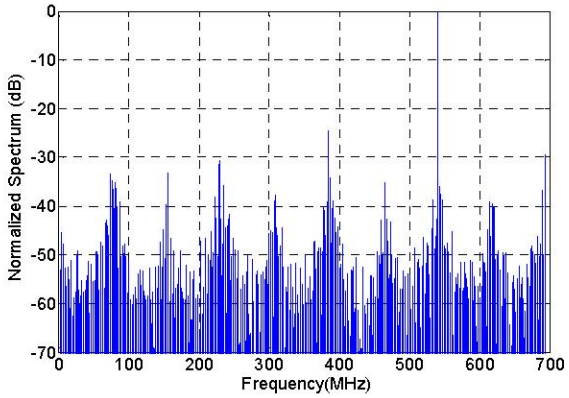

Fig. 12: Output spectrum for F_{in} = 540 MHz at F_s = 1400 MS/s

V. Conclusion

In this paper, we presented a 4-bit CMOS folding ADC architecture for DS-CDMA UWB transceivers. Two major design requirements were low power dissipation and a high sampling rate. To reduce the power consumption, we proposed a new architecture, which adopts an 8X folding amplifier. The 8X folding amplifier is implemented through multiplication of the outputs of two 4X folding amplifiers, which are also used to determine the third bit of the ADC. Our architecture saves two 4X folding amplifiers and two comparators at the cost of one additional analog multiplier compared with a traditional 4X folding ADC. The reduced hardware complexity of our ADC leads to low power dissipation. The high sampling rate is achieved by adopting current steering folding amplifiers instead of cross coupled differential pair based folding amplifiers.

The ADC was designed in 0.13 µm IBM CMOS process. Post-layout simulations indicate that our ADC achieves the required sampling rate of 1.4 GS/s and dissipates 62 mW with the supply voltage of 1.5 V. The SFDR of our ADC is greater than 24 dB up to 540 MHz at the sampling rate, and the INL and the DNL are less than 0.2 LSB and 0.3 LSB, respectively.

Table 1 summarizes the performance of the proposed ADC. The proposed ADC achieves a higher sampling rate than existing folding ADCs and maintains excellent linearity up to 540 MHz. The power consumption is reduced considerably compared to a conventional folding architecture, which is due to the reduction of the numbers of folding amplifiers and comparators in our ADC.

TABLE I: PERFORMANCE SUMMARY OF OUR ADC

Resolution	4 bits
Conversion Rate	1.4 GS/s
DNL	< 0.3 LSB
INL	< 0.2 LSB
SFDR (F_{in} = 20 MHz)	35 dB
SFDR (F_{in} = 540 MHz)	25 dB
Input Range	1Vpp (differential)
Supply Voltage	1.5V
Technology	0.13 µm CMOS process
Power consumption	62 mW
Input Impedance	50 Ω

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