Design of a 6-bit 5.4-Gsamples/s CMOS D/A Converter for DS-CDMA UWB transceivers

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***Abstract*—This paper presents a design of a 6-bit 5.4-Gsamples/s D/A converter in IBM 0.13 μm CMOS technology for DS-CDMA UWB transceivers. The high conversion rate and low supply voltage of 1.5 V make the design a challenge. To reduce the time constant of the circuit, we propose a two-stage current-steering topology, in which the distribution of the resistive and capacitive loads is balanced at the two stages. We also propose a folded-cascode current source cell that eliminates the need to control the crossing-points of the switch signals and minimizes the digital feedthrough. The current source cell does this without sacrificing headroom, so the circuit is suitable for a low supply voltage. Post-layout simulation has been performed to estimate performance. At the conversion rate of 5.4 Gsamples/s, the spurious free dynamic range (SFDR) is greater than 38 dB for three different signal frequencies. Both the integral nonlinearity (INL) and differential nonlinearity (DNL) stay within 0.3 LSB. The layout occupies a small active area of 110 μm × 90 μm, and the D/A converter consumes only 20 mW of power.**

***Index Terms*—CMOS, D/A converter, DAC, DS-CDMA, UWB, SFDR, INL, DNL, current-steering, folded-cascode, current source cell, feedthrough**

I. Introduction

For a DS-CDMA UWB transceiver, one practical approach for generation of the data signal is to use a high-speed low-resolution D/A converter followed by a low pass filter to shape the spectrum. Due to the hardware complexity of implementing a high-order filter, it is desirable to push the conversion rate of the D/A converter as high as possible. In the DS-CDMA UWB proposal, the highest data rate is 1.35 Gbps [1]. Four times oversampling of the data signal necessitates the D/A converter operate at 5.4 Gsamples/s.

A high conversion rate makes a D/A converter susceptible to parasitic capacitances of the circuit, which may cause digital feedthrough, weak isolation, significant glitch energy, and slow transient time. These result in a sharp drop in the spurious free dynamic range (SFDR). CMOS current-steering D/A converters are a commonly adopted architecture for modern communication systems. Many recent publications have revealed its success for high-resolution and relatively high-speed D/A converters [2]-[5]. A 10-bit 1-Gsamples/s current-steering D/A converter with a measured SFDR of better than 60dB has been achieved in [5]. Intensive research has been conducted to improve the dynamic performance of D/A converters at high frequency [6]-[10]. A return-to-zero strategy was utilized at the output stage to achieve low distortion [9]. A mathematical relationship between the resolution and the SFDR of a D/A converter determined by the second harmonic term was studied in [10], and the influence of the output impedance on the dynamic performance was also discussed in the paper. However, as the rising and falling transitions occupy a large percentage of a clock period, and the low supply voltage limits the number of the transistors stacked in series, these techniques become less effective or even unfeasible.

In spite of intensive research in high speed D/A converters, a *single* CMOS D/A converter with the conversion rate up to several Gsamples/s has not been reported yet. An 8 Gsamples/s D/A converter has been achieved by time interleaving eight D/A converters, each enabled by phase-shifted versions of a 1 GHz clock [11]. The drawback of this architecture is high circuit complexity, large power consumption, and high sensitivity to the edge of the clock signal. Therefore, the time-interleaved architecture is not pursued in our D/A converter design.

Instead, we aim for a smaller transition time or time constant, so we propose a two-stage current-steering topology in this paper. We suggest folded-cascode current source cells that relax the headroom constraint caused by a low supply voltage. They also minimize the feedthrough and glitches without employing a high-speed driver for the crossing-point control of the switch signals. Note that a conventional current source cell requires careful control of the crossing-points to avoid turning off both switch transistors simultaneously, so that the fluctuation on the drain voltage of the current source transistor is minimized.

The paper is organized as follows. In the next section, the proposed two-stage current-steering topology is presented. Based on equivalent circuit models, we compare the time constant of a two-stage topology with that of a single-stage topology. The effect of capacitive and resistive loads on the main pole of the circuit is also analyzed through MATLAB simulations. In Section III, the overall block diagram of our D/A converter is described, and the design of each building block is explained. Section IV presents post layout simulation results, and Section V draws a few conclusions from this work.

II. PROPOSED TOPOLOGY

D/A conversion can be accomplished through the scaling of a reference voltage, charge, or current. A voltage division scheme is generally realized through selecting different tap positions of a resistor ladder. Poor accuracy of resistors combined with the large delay due to the switching network and the following buffer stage make the voltage scaling method unfavorable to high-speed D/A converters [12]. A charge redistribution architecture is based on a set of capacitors, and it also suffers from low accuracy and low speed [13]. A current-steering topology employs a set of current source branches that are switched by the input signals. The advantage of a current-steering topology lies in its inherent high speed and its lack of an output buffer. However, as the conversion rate increases dramatically, the dynamic performance of a current-steering topology degrades significantly, as a larger percentage of the clock period is due to the rise and fall delay of the clock signal.

For a traditional single-stage current-steering D/A converter, the equivalent single-pole circuit model shown in Fig. 1 is often used for analyzing its transient behavior. The matching resistor R_m is equal to the load resistor R_o, and the equivalent resistor R is one half of R_o. C represents the parasitic capacitances at the output node, including the transistor junction capacitances and the interconnect parasitics at the output. The settling time for a single-stage D/A converter is proportional to the time constant $\tau_s = RC$. Since the load resistor R_o is usually given as a design specification, the output parasitic capacitance C should be minimized to reduce the settling time. For example, the capacitance C should be less than several pF for a GHz range D/A conversion under the output load resistance R_o = 100 Ω. Since all current source cells are connected to the output node, the total parasitic capacitance at the output node may exceed the allowable limit. Therefore, a straightforward approach alone to reduce the output parasitic capacitance would be insufficient to achieve high speed for current-steering D/A converters.

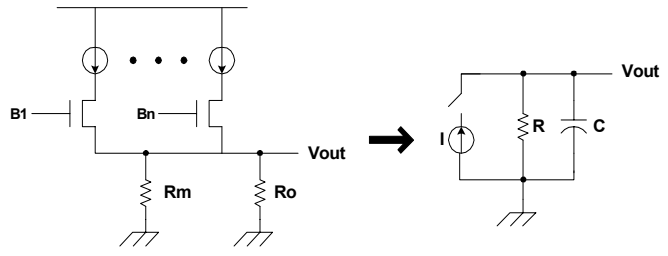

Fig.1: A single-stage current-steering topology and its equivalent circuit model

We, thereby, propose a two-stage current-steering topology to address the problem. The proposed topology consists of two current-steering D/A converters connected through a resistor, and its equivalent circuit is shown in Fig. 2. In the figure, R_x and C_x represent the resistance and the parasitic capacitance associated with an internal node X, and R_o and C_o with the output node. The advantage of the proposed two-stage topology is that the capacitive and resistive loads can be distributed over the two stages to improve the speed. We analyze the performance of the proposed two-stage topology in the following.

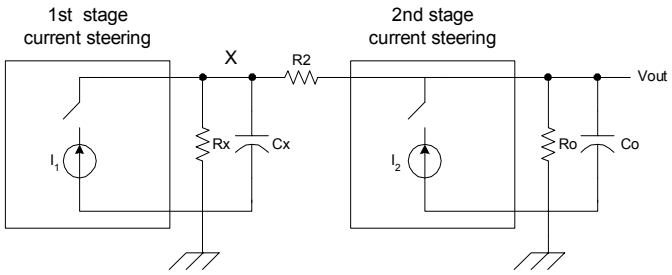

Fig. 2: The proposed two-stage current-steering topology

We have the following constraint for the resistive matching.

$$R_o = R_2 + R_x \tag{1}$$

The output peak-to-peak voltage swing ΔV_{out} is the difference between the two output voltages obtained with both current sources turned on and both turned off. Using (1), the output swing voltage is easily obtained as given in (2). Note that the output voltage swing is usually given as a design specification.

$$\Delta V_{out} = \frac{1}{2}\left(I_1 \cdot R_x + I_2 \cdot R_o\right) \tag{2}$$

Let us analyze the transient response of the proposed topology. Assuming I_1 and I_2 are step-functions, the output voltage can be expressed in the s domain as:

$$V_{out}(s) = \frac{I_1}{s} \cdot \frac{R_x R_o}{Xs^2 + Ys + Z} + \frac{I_2}{s} \cdot \frac{R_o(R_o + R_x R_2 C_x s)}{Xs^2 + Ys + Z} \tag{3}$$

where the constants X, Y and Z are

$$X = R_x R_2 R_o C_x C_o$$

$$Y = R_x R_o C_x + R_x R_2 C_x + R_o{}^2 C_o$$

$$Z = 2R_o$$

The poles of the two-stage topology, P_1 and P_2, can be written as:

$$P_1 = \frac{Y - \sqrt{\Delta}}{2X} \tag{4}$$

$$P_2 = \frac{Y + \sqrt{\Delta}}{2X} \tag{5}$$

where $\Delta = Y^2 - 4XZ = R_x^4 C_x^2 + 4R_2 R_x^3 C_x^2 + 2R_x^2 R_o^2 C_x C_o$

$$+ \left[2R_2 R_x C_x - R_o^2 C_o\right]^2 > 0$$

From the above expressions, both P_1 and P_2 are real numbers, so the system is overdamped. Obviously, the dominant or smaller pole P_1 dictates the time constant τ_t of the two-stage current-steering D/A converter.

Now, let us compare the time constant of the two-stage current-steering topology with that of the single-stage topology. The ratio of τ_s to τ_t is plotted as a function of R_x/R_o, and C_x/C in Fig. 3. It can be seen from the plot that the ratio can be maximized through a proper selection of R_x (= $R_o - R_2$) and C_x, i.e., the time constant for the two-stage current-steering topology can be minimized compared with that for the single-

stage topology. For a given C_x, as R_x decreases, the ratio of τ_s to τ_t increases at the cost of the reduced output swing voltage ΔV_{out} from (2). To maintain the output swing voltage, current I_1 should increase to trade speed for power. The distribution of parasitic capacitances over the two stages affects the overall speed, and the plot shows that a good configuration occurs when the two parasitic capacitances are approximately equal, as indicated as a dotted line.

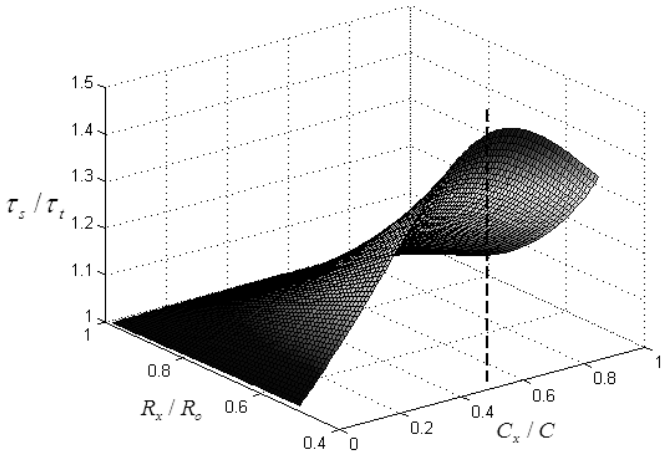

Fig. 3: Ratio of τ_s and τ_t as a function of R_x/R_o and C_x/C

III. CIRCUIT DESIGNS

Fig. 4 shows the block diagram of our 6-bit two-stage segmented current-steering D/A converter. The segmented architecture is often used to achieve good differential non-linearity (DNL) by minimizing the dynamic error due to the switch of the MSBs [5]. Two MSBs are converted to a 3-bit thermometer code, while the remaining four LSBs pass through delay elements to equalize the delays of all the bits. The two MSBs of the thermometer outputs are applied to the first stage, the LSB of the thermometer and the four bits, B_3 through B_6, to the second stage. The seven bits are divided over the two stages to make the parasitic capacitances approximately equal on the outputs of the two stages. Since a higher order bit carries a higher level of current to incur larger parasitic capacitance, a smaller number of MSBs is assigned to the first stage. The design of each building block is explained in the following.

A. Analog Circuitry

The key building block of a current-steering D/A converter is a current source cell. The basic structure of a current source cell is shown in Fig. 5. It could be implemented with either NMOS or PMOS transistors. Transistor M1 supplies the required current, and the differential input signals switch M2 and M3 accordingly to steer the current through the load resistors. Assuming a matched resistive load, the output voltage V_{out} of the NMOS-based cell varies from $V_{dd}/2 - \Delta V_{out}$ to $V_{dd}/2$, as the output voltage is shared equally by the two resistors, R_m and the load resistor, when all the switches are off. So the available headroom for the two stacked transistors is limited to $V_{dd}/2 - \Delta V_{out}$. The limited headroom is problematic for a low supply voltage to guarantee that the transistors operate in the saturation region. For the PMOS-based cell, on the other hand, there is no voltage drop on the load resistor when all the switches are off. Therefore, the available headroom for two stacked transistors increases to $V_{dd} - \Delta V_{out}$. Furthermore, the n-well in which the PMOS device is built on provides a good shield from a nearby digital circuit. Therefore, a PMOS-based cell is chosen for our design.

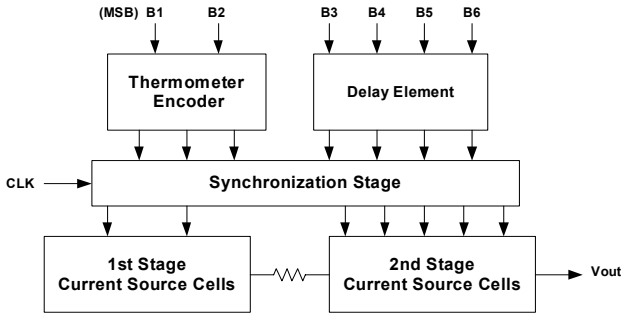

Fig. 4: Block diagram of our 6-bit two-stage segmented D/A converter

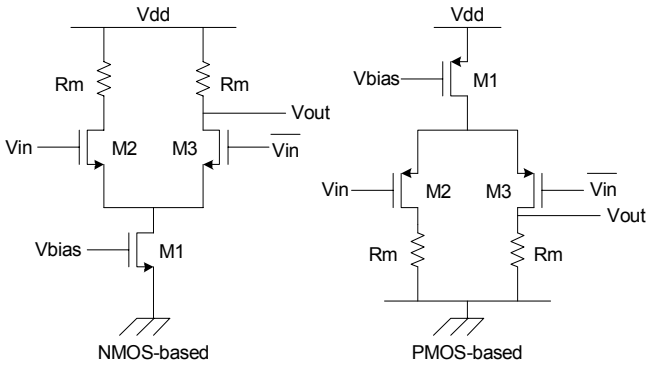

Fig. 5: Basic current source cells

A drawback of the basic PMOS-based current source cell in Fig. 5 is its poor dynamic performance caused by the digital input signal feedthrough due to the gate-to-drain parasitic capacitance of a switch transistor. Lowering the voltage swing of the input signals is one way to reduce the glitch energy. However, it is not suitable for our design because the reduction of the voltage swing decreases speed of the digital circuitry significantly. Another scheme is to add cascode transistors M4 and M5 below the switch transistors as shown in Fig. 6. Van den Bosch et al. showed improvement of the dynamic performance for the circuit [10]. However, the applicability of this configuration for low-supply high-speed D/A converters becomes problematic. First, the overdrive voltage of transistors is reduced to require larger transistors, which results in larger parasitic capacitance. Second, more importantly, we should not turn off the switch transistors M2 and M3 simultaneously for both basic and cascode current source cells, which requires a careful control of the crossing-points of the differential input signals. Designing such a driver

could be very challenging for high-speed D/A converters.

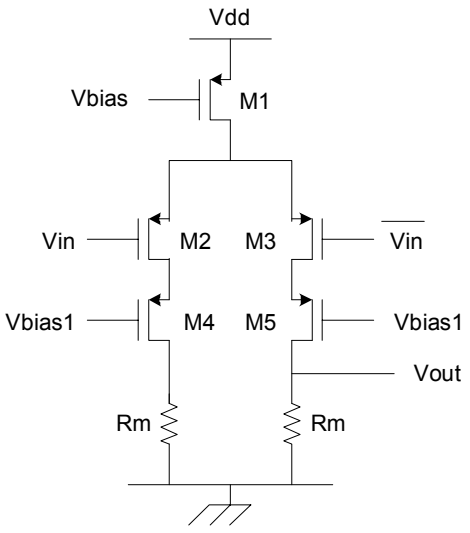

Fig. 6: Cascode current source cell

We propose a folded-cascode current source cell as shown in Fig. 7 for our high speed D/A converter. By using an NMOS transistor as a switch in parallel with the PMOS transistor, the digital input feedthrough can be reduced without reducing the headroom. The transistor M2 provides isolation between the input and the output, as the transistors M4 and M5 do in the cascode current source cell. Also, it boosts the output impedance seen from the output node into the drain of the transistor. The single-ended output shown in the figure does not need differential input signals to eliminate the need for a sophisticated control of crossing-points, and it is also true for differential inputs. In addition, the input signal can have a full swing, which is desirable to increase the speed of the digital circuitry. All of these advantages make the folded-cascode current source cell an excellent choice for low-voltage high-speed D/A converters. The only disadvantage is that a differential output requires two current cells, which doubles the power dissipation as well as the circuit complexity.

The accuracy of the current sources depends on the transistor sizing, overdrive voltage, and the mismatch process parameters. A relation is formulated in [14] as:

$$\left(\frac{\sigma(I)}{I}\right)^2 = \frac{1}{2W_{CS}L_{CS}}\left(A_\beta^2 + \frac{4A_{VT}^2}{V_{OD\_CS}{}^2}\right) \tag{6}$$

where $\sigma(I)/I$ represents the relative standard deviation of a current source, W_{CS} and L_{CS} are the width and length of the current source transistor, A_β and A_{VT} are mismatch process constants, respectively, and V_{OD_CS} is the overdrive voltage of the current source transistor. Generally speaking, larger transistor size and higher overdrive voltage are preferable for higher accuracy, but they are limited by parasitic capacitances and the available voltage headroom.

Van den Bosch et al. related the required accuracy of current sources to the yield as [15]

$$\frac{\sigma(I)}{I} \le \frac{1}{2C\sqrt{2^N}} \text{ with } C = inv\_norm\left(0.5 + \frac{yield}{2}\right) \tag{7}$$

where N is the resolution of the D/A converter, *inv_norm* stands for inverse cumulative normal distribution. To achieve a certain yield, the specification for the accuracy of the current sources can be determined.

The two expressions (6) and (7) are useful guidelines to design current source transistors.

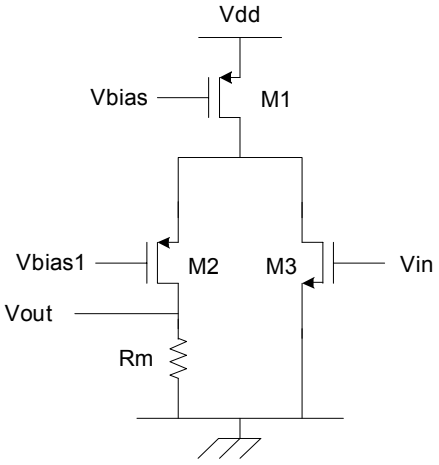

Fig. 7: Folded-cascode current cell

B. Digital Circuitry

All the digital blocks were designed manually instead of using standard cells in order to achieve high speed. The binary-to-thermometer encoder was implemented with inverters, two-input NAND and NOR gates, and the delay element was implemented with a number of inverters. The synchronization of the input signals to the current source cells is achieved by placing edge-triggered Transmission Gate (TG)-based flip-flops in front of the switches and the flip-flop used for our design is shown in Fig. 8 [16]. Finally, we added six 4-to-1 digital multiplexors at the inputs for the purpose of testing our standalone D/A converter, which reduced the data rate of the test inputs by four times.

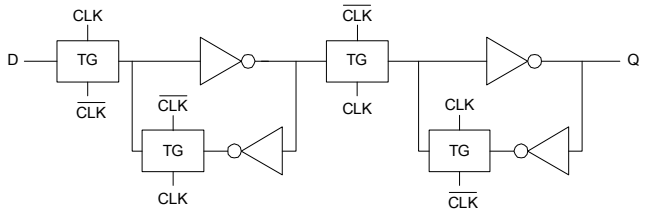

Fig.8: A TG-based flip-flop

IV. Post-layout simulation results

The proposed 6-bit 5.4 Gsamples/s D/A converter was laid out in IBM 0.13 μm CMOS technology. The core layout is shown in Fig. 9. In order to minimize cross talk between the analog and digital circuit blocks, we used separate power supplies for the two blocks and placed guard rings around the

analog block. The post-layout simulations were performed without considering process variations.

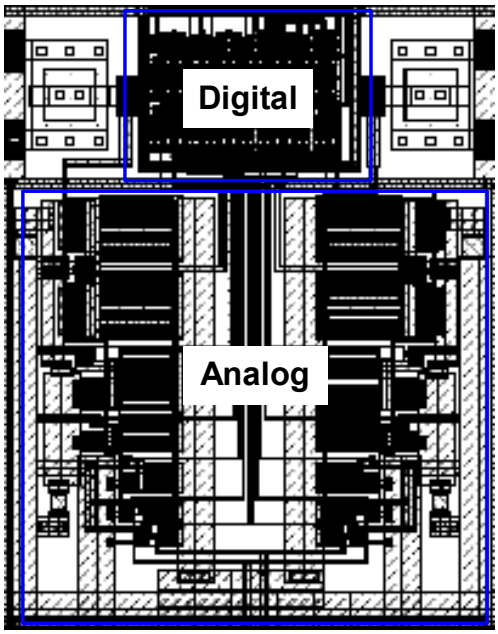

Fig. 9: Core part of a 6-bit 5.4 Gsamples/s D/A converter

The simulated integral non-linearity (INL) and differential non-linearity (DNL) versus input codes are shown in Fig. 10 and Fig. 11, respectively. It can be seen that both INL and DNL are smaller than 0.3 LSB for the entire range of the input code. The spurious free dynamic range (SFDR) was simulated for three different signal frequencies, 1.35 GHz, 675 MHz, and 337.5 MHz, at the conversion rate of 5.4 Gsamples/s. The SFDR is greater than 38.5 dB for the input signal frequency of 1.35GHz, greater than 43.9 dB for 675 MHz, and greater than 47 dB for 337.5 MHz. As expected, the SFDR increases as the signal frequency decreases. Table 1 summarizes the simulated performance of our D/A converter.

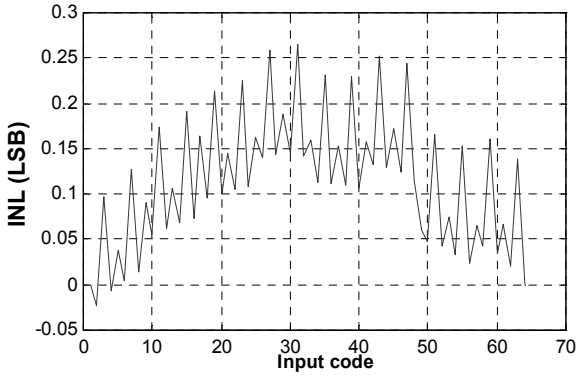

Fig. 10: Simulated INL versus input codes

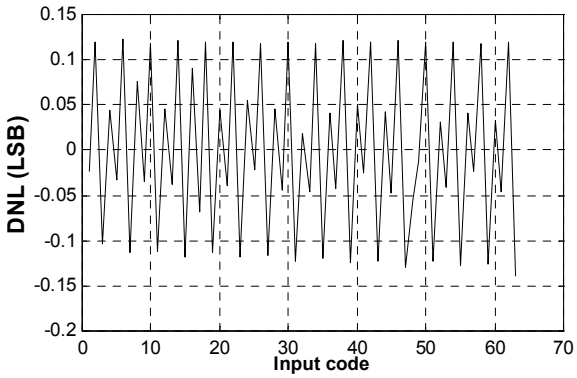

Fig. 11: Simulated DNL versus input codes

TABLE 1. SUMMARY OF POST-LAYOUT SIMULATION PERFORMANCE

Process	IBM 0.13 µm CMOS
Resolution	6 bit
Conversion Rate	5.4 Gsamples/s
INL	< 0.26 LSB
DNL	< 0.15 LSB
SFDR	> 38.5 dB (1.35GHz@5.4 GS/s) > 43.9 dB (675MHz@5.4 GS/s) > 47 dB (337.5MHz@5.4 GS/s)
Output Impedance	100 Ω
Power Consumption	20 mW
Active area	110 µm x 90 µm

V. CONCLUSION

In this paper, we presented a 6-bit 5.4-Gsamples/s D/A converter in IBM 0.13 µm CMOS technology for DS-CDMA UWB transceivers. In order to achieve a high sampling frequency, we proposed a two-stage current-steering topology. Our analysis shows that if the capacitive and resistive loads are equally distributed over the two stages, the time constant of the dominant pole can be reduced to result in a faster transition time. To ease high-speed digital design at a low supply voltage, we proposed folded-cascode current source cells. The performance of our D/A converter was estimated through post-layout simulations. The simulation results show that the INL is smaller than 0.3 LSB for the entire range of the input code and the SFDR is greater than 38 dB for the three input signal frequencies considered.

In conclusion, our D/A converter is the first single CMOS D/A converter that can operate up to 5.4 Gsamples/s, while achieving good dynamic and linearity performance.

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