Dual Use of Power Lines for Data Communications in a System-On-Chip Environment

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Abstract—**We propose to use power pins to simultaneously carry data signals while delivering its power. A direct superposition of a data signal on a power pin would fail due to an inherent high noise level on power lines and precludes the possibility for multiple data channels. To address the problem, we suggest adoption of the UWB (Ultra Wideband) and direct sequence-code division multiple access (DS-CDMA) communication technologies. Because of the wide bandwidth, a UWB signal can reduce its average power level practically to the noise level. The DS-CDMA further mitigates the noise and allows multiple data channels to share inter-connected power lines. We studied the feasibility of the proposed scheme through SPICE simulations and present the simulation results.**

I. Introduction

Power line communications, which are ubiquitous, intends to dual use of power lines, data communications and delivery of power [1], [2]. When the scope is down into VLSI chips or PCBs, it can be realized that the environment is essentially the same. Power lines of a chip or a PCB could be used inter- and intra-chip data communications. In this paper, we investigate the feasibility for dual use of power lines in a VLSI chip environment.

The number of pins on a VLSI chip seems to grow boundlessly with advancement of VLSI technology into a deeper submicron technology. The increasing pin count results not only from additional signal pins but also from additional power and ground pins. For example, the Intel Pentium 4 processor in the 775-land package has a total of 775 pins (lands), of which 226 pins are for power and 274 pins for ground. Additional pins increase the cost of a chip and lead to a larger footprint. We propose to investigate the possibility of using power pins to carry data signals while serving their intended purpose, supply of power. The dual use of the power pins can significantly reduce the pin count, size, and hence the cost of a chip.

The organization of the paper is as follows: Section II presents technical problems posed for dual use of power pins, Section III describes principles behind the proposed research mainly consisting of ultra wideband (UWB) and DS-CDMA (Direct Sequence-Code Division Multiple Access), Section IV shows the modeling and simulations, and Section V conclusions with suggested future works.

II. Problem Statements and Motivations

We investigated the feasibility of using power pins and power distribution networks for simultaneously carrying data and delivering power. A direct superposition of a data signal on a power pin does not permit simultaneous use for data and power. The data signal induces undesired fluctuations in the power line voltage, and high noise levels in the power lines corrupt the signal. Further, the direct supposition precludes the possibility of multiple data channels on power lines.

Cellular wireless communications faces essentially the same problems; the channel is noisy and should be shared by multiple users. A pervasive scheme used in the second and third generation wireless communications is CDMA [3], [4], and we propose to adopt the same scheme, more specifically, UWB and DS-CDMA. Owing to its wide bandwidth, UWB offers high data rate with average power near the noise level. DS-CDMA is an effective method to mitigate the high noise level while providing a method for multiple data channels.

Since FCC's allocation of a UWB spectrum in 2002, UWB has gained phenomenal interest in academia and industry. Compared to traditional narrowband communication systems, UWB has several advantages such as high data rate, low average power, and simple RF circuit. Many of these potential advantages are a direct consequence of the large instantaneous bandwidth, which is on the order of several GHz. UWB signals overlay existing spectrum, but their low power limits the impact to the underlying signals. UWB signaling can be carrier-based or impulse-based, and the impulse-based signaling is more suitable for the proposed application due to its simple hardware.

The DS-CDMA technology assigns a codeword to each bit of information called spreading, and the orthogonal codewords are assigned to different users. We describe the spreading operation and benefits of the DS-CDMA technology in more detail. The spreading operation represents one bit of data as a series of binary (positive and negative) pulses spread over a codeword. For example, a codeword of {1, 1, -1, -1} represents a data bit {1} and the opposite, {-1, -1, 1, 1}, a data bit {0}. To send one bit of information, we have to send four pulses, which either reduces the data rate or increases the pulse repetition

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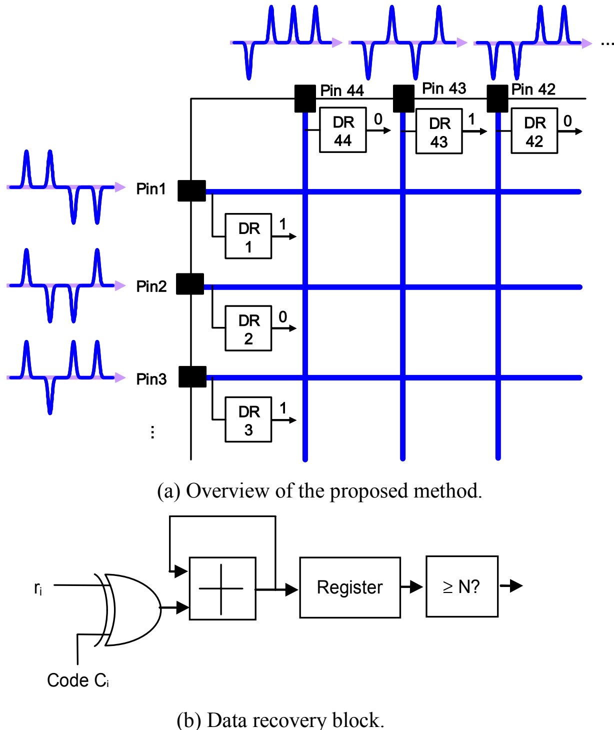
frequency. The benefit of the spreading operation is the processing gain, which is *10*log* (*spreading_factor*) in dB. For the example 4-bit codeword, the spreading factor is 4, which yields a processing gain of 6 dB. This implies that the signal power of the pulses can be reduced by 6 dB, while maintaining the same signal-to-noise ratio. Thus, DS-CDMA further reduces the impact of UWB pulses on power line fluctuations, and the de-spreading operation permits better recovery of the signal.

III. PROPOSED APPROACH

Two major technical challenges exist for the proposed method. The first one is to reduce the impact of fluctuations caused by the data signal applied on a power pin, while the signal is recoverable from the power distribution network. The second one is to enable multiple data transmissions on multiple power pins. As noted earlier, we propose to employ UWB and DS-CDMA communication techniques to address the challenges.

Fig. 1 illustrates the proposed method on a package with 44 power pins and a circuit diagram for a data recovery block DR *i*. One bit of information is spread over multiple, narrow UWB pulses (which are typically a few hundreds picoseconds wide) called chips. Antipodal binary-phase modulation is adopted in the figure, in which a chip signal represents logic {1} ({0}) as a positive (negative) pulse. UWB pulses are observed at the output of the power pad. A data recovery block, which is an accumulator, de-spreads the received signal to recover the data bit. A data recovery block may not require any analog RF components except a simple comparator on its input.



(a) Overview of the proposed method.

(b) Data recovery block.

Figure 1. Application of data signals to power pins

The next challenge is to enable multiple data transmissions on power pins. Since all power lines are electrically connected inside a chip, multiple data signals on power lines interfere with each other. The DS-CDMA technique is employed to address this problem. When orthogonal codes are assigned to those multiple data channels, all the other data signals except the intended one behave as noise through the de-spreading operation. For example, a codeword {1, 1, -1, -1} is assigned on pin 1, while a codeword {1, -1, -1, 1} on pin 2. The data recovery block associated with pin 1 de-spreads the received signal with the corresponding code ({1, 1, -1, -1}). When a data bit {1} is applied to pin 1, the de-spread value becomes 4 in a noise-free environment. When the data signal from pin 2 is de-spread by the same data recovery block, the de-spread value becomes 0, ignoring the slight difference in the propagation delays of the two signals. This means the data signals from other pins do not interfere with the data recovery from a desired power pin. In reality, this is not true due to imperfect orthogonality caused by noise and propagation delay differences.

IV. MODELING AND SIMULATION RESULTS

In order to investigate the feasibility of the proposed method, we modeled an IC package and a power distribution network and simulated the proposed system. The IC package considers wire bonds and lead frames, and power pads including a diode for electrostatic discharge (ESD). A power distribution network is a mesh of conducting lines.

A. Package and Power Pad Model

A widely adopted model for an IC package and a power pad is shown in Fig. 2 [5]. V_i is the applied voltage of a pin, and V_o is the output voltage of the power pad. L_0, C_0, and R_0 are the parasitics of the package associated with wire bonds and lead frames, and C_1 and R_1 are the parasitics of the power pad. R_L represents the power distribution network, which is explained in detail in the following. Note that parasitics of L_0, C_0, and R_0 are usually provided by the packaging company.

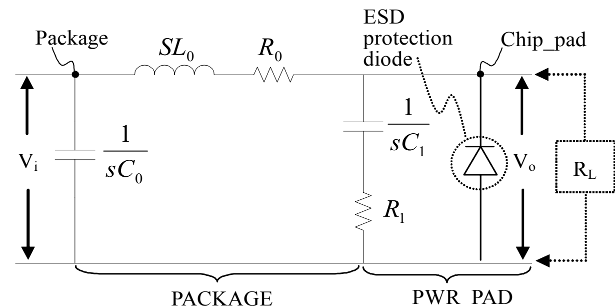


Figure 2. An equivalent circuit of a package and a power pad

We considered an Amkor flexBGA 144 pin package for our simulation due to the availability of its parasitic values in the public domain [7], and the following parameters are used.

- Parasitics of the package: L_0 = 0.25 nH, C_0 = 0.13 pF, and R_0 = 5 mΩ
- Parasitics of the power pad: C_1 = 203.62 fF and R_1 = 5 Ω
- ESD protection diode: (W/L=297/4), M=16. The diode consists of 16 NMOS devices in parallel. The width of an NMOS diode is 35.64 μm and the length of 0.48 μm,

The capacitive parasitics C_1 of a power pad is based on TSMC 0.25 μm deep submicron process. The resistive parasitics R_1 is calculated from the sheet resistance model [8]. The capacitive parasitics of the ESD protection diode is extracted from the layout of the power pad.

B. Power Distribution Network Model

An on-chip power distribution network can be modeled as series and parallel connections of R, L, and C networks [9]. We adopt an *N*-stage ∏-type distributed RLC model, and Fig. 3 illustrates the model for *N*=3. The current sources model the current consumed by the devices, and they are evenly distributed over the entire network. As shown in Figure 4, the row or column for an *N*-stage model consists of *N* resistors with R/*N* Ω each, the two end-capacitors with C/2*N* farads each, and the rest (*N*-1) capacitors with C/*N* farads.

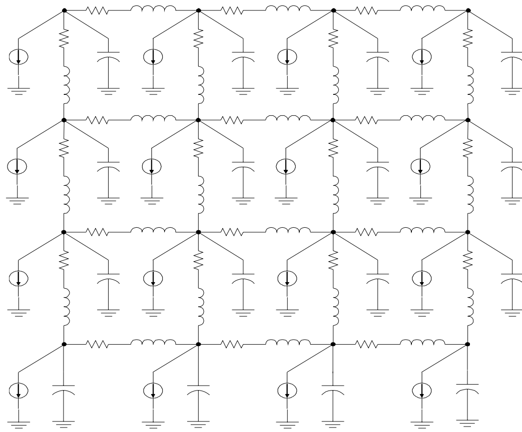


Figure 3. A *3*-stage ∏-type power distribution network model.

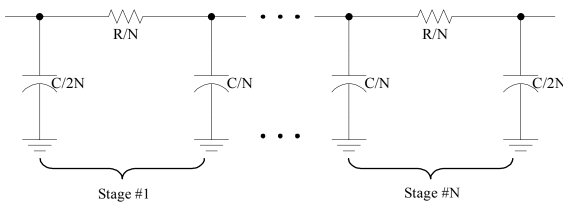


Figure 4. An *N*-stage ∏-type distributed RLC model.

The number of stages *N* is set to 12 for our model, as it is sufficiently accurate for the delay estimation [6]. Our power distribution network is modeled for an IBM PowerPC750 processor in BGA (Ball Grid Array) package. The dimension of our power distribution network is set to 8.79 mm × 8.79 mm based on the area of the PowerPC chip (which is 7.56 mm × 8.79 mm). The dynamic power consumption of the processor is 7.3 W @ 300 MHz with the supply voltage of 2.5V. The current source I_s at each cross point sinks 17.6 mA to result in the total power consumption of 7.3 W. The maximum IR resistive drop is set to 10 percents of the power supply voltage, which is 0.25 V at the center point of the grid. We computed the width of a power line *w* to achieve the maximum allowable IR drop.

The inductive parasitics was obtained using the following equation [5].

$$L = \frac{\mu}{2\pi} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right)$$

where *w* = width of a power line, $h = t_{ox}+t_{Si}$. Since the thickness of the Si substrate is about 250 μm and that of the oxide is 5.8 nm, *h* is approximated to t_{Si}, i.e., 250 μm. Finally, the PowerPC processor has 93 power/ground pins out of 360 pins, and the total number of power pins is set to 44 for our simulation.

C. Simulation

Gaussian UWB pulses with the peak amplitude of 0.25 V, (i.e., 10 percents of the supply voltage) and the width of 1 ns were considered for our simulation. The maximum chipping rate (i.e., the raw data rate) for the Gaussian pulses is 1 GHz.

The first and most critical experiment is to examine whether UWB pulses propagate through power pins. We applied UWB pulses only at power Pin 1 (refer to Fig. 1.), while the rest of the 43 power pins are at VDD = 2.5 V. Fig. 5 shows the waveforms at the input of the power pin and at the output of the power pad (i.e. at the input of the data recovery block). The waveforms indicate that the peak attenuation of the pulses due to the package is 44 %, and the propagation delay is about 117 ps. Hence, it opens the possibility of using UWB pulses on power pins.

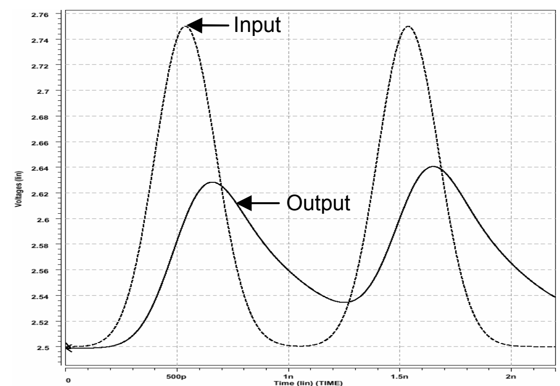


Figure 5. Waveforms at the input of a power pin and the output of the power pad

The next experiment is to examine the interference level from a UWB pulse applied to a pin to another pulse applied to an adjacent pin. We applied two consecutive positive pulses to Pin 5 and a positive pulse followed by a negative pulse at Pin 7. Note that Pin 6 is the center power pin on a side. Fig. 6 shows simulation results, and the output

waveform is shown only for Pin 5. As expected, when the two pulses are added constructively, the output increases. When two pulses have the opposite polarity as in the case of the second pulses, they are added destructively to maximize the interference. However, the attenuation level due to the interference is insignificant as shown in the figure, so the interference from other pins does not pose a problem. It is important to note that if a data recovery block moves away from the power pad, the level of interference will increase.

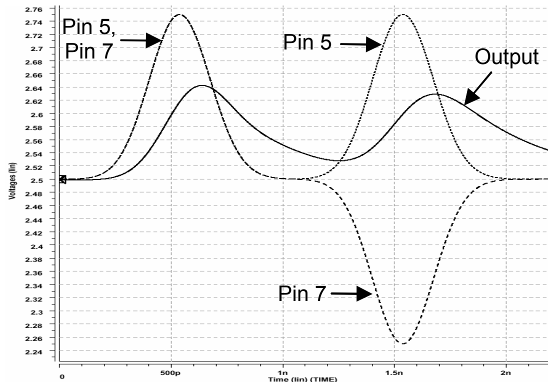


Figure 6. Waveforms at package power pins and at the power pad output.

So far, our simulations are limited to a noise free environment. Two noise sources, simultaneous switching noise (SSN) and thermal noise, are most significant for power distribution networks. We added SSN with the rising slope of 108 mA/ns for 50 ps followed by the symmetry falling slope to each current source and the repetition frequency of the SSN is 1 GHz. The top waveform in Fig. 7 is the waveform of the SSN, and the bottom one is input and output waveforms on Pin 5 and Pin 7. The output waveform has a notch at the occurrence of the SSN. So the output waveform should not be sampled at the vicinity of the occurrence of the SSN.

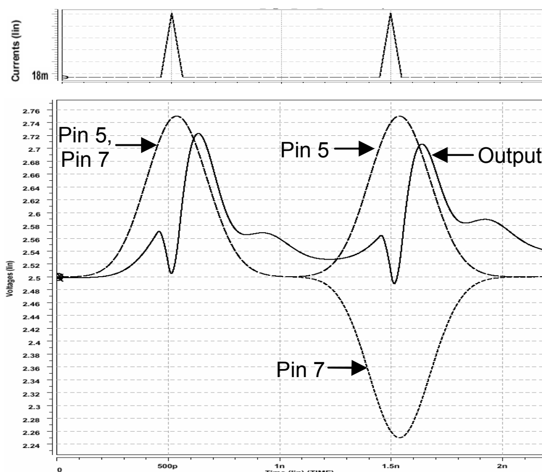


Figure 7. Waveforms at power pins and at the power pad output with the SSN of 1 GHz.

The final simulation is to add both SSN and the thermal noise. We added the two types of the noise to the current sources, and Fig. 8 shows the waveforms at SNR (Signal-to-Noise Ratio) of 10 dB. Although the waveform wiggles, the presence of the signal is manifest. The de-spreading operation employed primary for multiple data channels increases the SNR effectively. Other measures such as correlation and oversampling can be applied to recover the data.

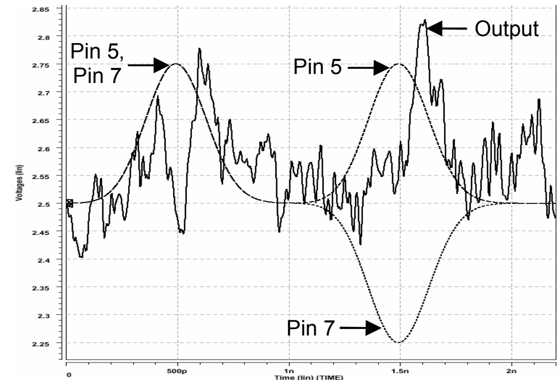


Figure 8. Waveforms at power pins and at the power pad output with the SSN of 1 GHz at SNR of 10 dB.

V. Conclusion

In this paper, we presented the feasibility for dual use of power pins, data communications as well as its intended purpose of delivery of power, based on the ultra wideband communication technology and the direct-sequence code division multiple access scheme. Our simulation results indicate that the proposed approach is quite feasible and can be applied to existing packages without or little modification. Further research including design of data recovery blocks and determination of various design parameters is necessary to deploy the proposed method to real world chips.

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