A Low-power CMOS Power Amplifier for Ultra wideband (UWB) Applications

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Abstract— This paper presents the design and implementation of a wideband power amplifier for UWB applications, covering the lower band frequencies of 3.1 GHz to 4.8 GHz. To achieve sufficient linearity and efficiency, this PA operates in the Class-AB regime, delivering an output power of -4.2 dBm at an input-1dB compression point of -22 dBm for a 4 GHz signal. This PA has a differential input and a single-ended output that has been matched to 50Ω at both the ends. Complete design and implementation was done using TSMC 0.18µm CMOS technology and it consumes a very low power of 25 mW, while realizing a flat gain of 19 ± 1 dB across the whole band of operation.

Index Terms: CMOS, power amplifier, UWB, low power, RF transceivers.

I. INTRODUCTION

Ever since the FCC allocated 7.5 GHz (from 3.1 GHz to 10.6 GHz) for ultra wideband (UWB) technology [1], interest has been renewed in both academic and industrial circles to exploit this vast spectrum for short range, high data rate wireless applications. The great potential of UWB lies in the fact that it can co-exist with the already licensed spectrum users and can still pave the way for a wide range of applications.

However, this wide bandwidth complicates the circuit level implementation of key RF blocks like the power amplifier (PA), transmit/receive switch, low noise amplifier (LNA) and mixers in an UWB transceiver. Though expensive technologies like SiGe or GaAs have been used for transceiver realizations, the ultimate goal is to have a single-chip, low-cost solution which can only be achieved by using CMOS technology. It has been shown that there is an improvement of only 1 dB in the link margin for spectrum above 4.8 GHz using existing CMOS technologies [2]. For circuit realizations above 4.8 GHz, this improvement comes at a disproportionately higher circuit complexity and higher power consumption. Hence designers are focusing on RF circuits that operate in the lower frequency band up to 4.8 GHz before technology improvements can enable the use of higher frequencies.

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A fully integrated CMOS power amplifier which can operate in the frequency range of 3.1 GHz to 4.8 GHz is described in this paper. This PA uses a feedback approach with cascode topology to realize the wideband specifications including matching and gain flatness. A complete design methodology for the design of the feedback network for any RF circuit is also described. Since the output power level of UWB signals must be low in order to prevent interference with the already existing technologies, the PA can be designed with smaller transistors and hence lower power consumption. Additionally, power control has also been integrated in the design.

Section II describes wideband impedance matching techniques along with an analysis of a source degenerated amplifier with feedback configuration. Section III discusses some of the implemented circuit details and section IV describes the simulation results.

II. DESIGN APPROACH

A. Wideband matching techniques

Typical narrowband applications use LC based networks to achieve matching at a particular frequency by exploiting the fact that the impedance of the network is resistive at the resonant frequency. Using filter theory, this approach can be extended for wideband matching conditions [3], [4]. However, when die area is limited, it is imperative that some performance metric be sacrificed for area. This is especially true for broadband matching because multiple LC stages might be needed and they can occupy a substantial die area.

Distributed amplifiers are also quite common for broadband circuit realizations [5]. Though good linearity and matching can be achieved over a wideband of frequencies, the power consumption and area occupied by these circuits can be quite high.

Another approach is to use a shunt feedback network (Fig. 1) usually comprising a resistor [6]. In this configuration the feedback network can be designed in such a way that it can provide the required match at both the input and output ends. This topology has the added advantage of providing stability to the amplifier and in achieving flat gain response.



Figure 1. Resistive shunt feedback for broadband matching.

For a transistor stage with gain A_{ν} , the input resistance can be shown to be

$$R_{in} = \frac{R_F}{1 + A_v} \tag{1}$$

The value of the feedback resistance R_F has to be selected according to the matching and gain requirements of the amplifier. A small R_F can provide excellent matching but the gain of the amplifier drops due to significant signal feedback through this path. On the other hand, a large R_F can provide good gain but reduces the effect of feedback. Through careful simulations, the optimum value of R_F can be achieved for the best matching and gain conditions.

B. Determination of feedback components

When the bandwidth requirements are really large, a straight-forward feedback resistor might not meet the requirements easily. Instead, some combination of passive/active elements might be needed in the feedback path.

Consider a practical common-source stage including the bond-wire inductance to ground that acts as source degeneration. The small-signal model of such a stage is shown in Fig.2.



Figure 2. Small signal model of a common-source stage.

If the feedback network Z_f is included, the small signal equivalent can be redrawn as in Fig. 3, where

$$Z'_{in} = sL_{bond} + \frac{1}{sC_{gs}} + \frac{g_m L_{bond}}{C_{gs} + C_{gd}}$$
(2)

$$g_{m,eff} = \frac{g_m v_{gs}}{v_{in}} = \frac{g_m}{1 + sg_m L_{band}}$$
(3)



Figure 3. Feedback configuration.

For this configuration, the input and output impedances and the gain can be calculated to be

$$Z_{in,o} = \frac{Z'_{in} Z_f}{Z_f + (A_v - 1)Z'_{in}}$$
(4)

$$Z_{out,o} = \frac{Z_f + (R_s \parallel Z'_{in})}{1 + g_{m,eff}(R_s \parallel Z'_{in})}$$
(5)

$$A_{\nu} = \frac{R_L + g_{m,eff} Z_f R_L}{R_I - Z_f} \tag{6}$$

For a specified gain and impedance, plots of Z_f can be drawn at the desired frequency range of interest. Since the circuit parameters Z'_{in} and $g_{m,eff}$ are frequency dependant, the characteristics of Z_f will also vary accordingly over the frequency band. If the Z_f plot can be reproduced using some combination of R, L or C components, perfect matching and gain conditions can be achieved.

However, when designing for low noise or low power, the optimal solution for the feedback network can be realized only by tuning some of the circuit/transistor parameters and by iterating the above procedure. Various R,L,C combinations can reproduce the same Z_f characteristics, but the trade-off between power, noise, gain and impedance match will eventually determine the best feedback network.

III. CIRCUIT DESIGN DETAILS

A. Design Topologies

In an integrated transceiver, power amplifiers are usually preceded by an up-conversion mixer and followed by a T/R switch. Typically, mixer outputs are differential because of the inherent advantages of differential topologies like good isolation and noise immunity. Therefore the PA has to take differential inputs from the mixer and produce a single ended output to the T/R switch.

Two different design approaches for a differential input-single ended output amplifier are shown in Fig. 4.



(b) Design-2

Figure 4. Realizations of differential input-single ended output PA.

In design-1, the differential input is first converted to a single ended signal and then amplified. However, using separate power amplifiers for each single ended input relaxes the gain and linearity requirements on each of these PAs when compared to using a single PA. This technique shown as design-2 in Fig. 4(b) was used to realize our UWB PA.

B. Schematic and layout

Fig. 5 shows the schematic of the input stage of our UWB PA implemented using design-2 topology. This stage employs a cascode configuration and it operates in class-AB region. Input matching was realized using a series R-C feedback network, designed as described in section II. Since UWB systems have a very low power budget, it is imperative that there be no signal loss from the mixer and hence the input of the PA and the output of the mixer will have to be matched internally. Additionally, to aid in testing purposes and to accommodate the use of an external mixer if necessary, we decided to match the input of the PA to 50 Ω over the entire bandwidth.



Figure 5. Simplified PA schematic (Input stage).

To conserve battery power when not in operation, a power down switch M3, controlled by an external control signal V_Cntrl has also been included in the design. This transistor is implemented as a large PMOS transistor so that there is very little voltage drop across it when turned on.

The differential-to-single converter following the PA stages was realized using a differential amplifier with a current mirror load [7].

Fig. 6 shows the micrograph of the PA (1.9mm x 1.1mm) fabricated in TSMC 0.18 μ m CMOS technology. Our design integrates the input-output matching network, inter-stage matching, bias resistors, ac decoupling capacitors and even large RFC's (RF chokes) within the chip and hence is ideal for being a part of a complete transceiver implementation. Measurements on this chip are yet to be taken.

IV. RESULTS

In this section we summarize the simulation results of the PA performed using SpectreRF. Small signal gain and matching observed using S-parameter analysis is shown in Fig. 7. The overall system gain is 19dB with a flatness of ± 1 dB across the frequency band from 3.1 GHz to 4.8 GHz. The return loss at the input and output is less than -10 dB and -8 dB respectively. The power amplifier draws a very low power of 25mW from a supply of 1.8 V. Periodic steady state (PSS) simulations show an input 1-dB compression at -21.7 dBm for a 4 GHz signal and the PA delivers an output of -4.2 dBm at this point (Fig. 8).

It should be mentioned that real UWB type signals have minute voltage swing levels and hence non-linear effects would be minimal which has not been considered in our simulations. Another noteworthy characteristic about UWB PAs is that since it is a low output power circuit, bandwidth is the real problem and efficiency is hardly an issue.



Figure 6. Die Micrograph



Figure 7. Matching and small signal gain.



Figure 8. Input Power versus Output Power.

TABLE I. PERFORMANCE SUMMARY

Categories	Specifications	Units
Supply voltage	1.8	V
Frequency range	3.1 ~ 4.8	GHz
Output P1dB	-4.2	dBm
Input P1dB	-22.0	dBm
Gain	19±1	dB
S11	< -10	dB
S22	< -8	dB
Power Consumption	25	mW

V. CONCLUSION

We have presented the design and implementation of a CMOS power amplifier in TSMC 0.18µm technology that can be targeted for UWB applications. The frequency band of interest is 3. 1GHz to 4.8 GHz and the output power delivered to a 50 Ω load is -4.2 dBm at 4 GHz. This power amplifier is a low-power design consuming only 25mW from a 1.8 V supply, and providing a gain of 19±1 dB. Unlike distributed power amplifiers, this PA consumes very little power and is ideal for UWB transceiver implementations. With better technology, our design methodology can be extended for use up to 10.6 GHz in the future.

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