A Systematic Approach to CMOS Low Noise Amplifier Design for Ultrawideband Applications

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***Abstract*— In this paper, we introduce a systematic method to design CMOS low noise amplifier (LNA) for ultrawideband (UWB) applications. The proposed method is addressed to optimize noise performance and power efficiency while maintaining good input and output matching. The synthesized LNA achieves up to 14dB power gain with a low noise figure (NF) of 2dB and provides a reasonably acceptable input and output matching of -10dB across the frequency range of 3~5*GHz*. The developed LNA, implemented in TSMC 0.18*μm* CMOS technology, is single-stage architecture with very low power dissipation of 9*mW* with 0.9*V* supply.**

I. INTRODUCTION

Ever since RF CMOS technology was introduced, the major difficulties of RF CMOS circuit implementation are relatively lower unity-gain-frequency and poor noise performance of CMOS technology. In fact, the bigger problem is the lack of systematical design procedure for RF CMOS circuit implementation. Recently reported ultrawideband (UWB) CMOS LNA design can be found in [1]. The LNA introduced in [1] employs a *Chebyshev* filter configuration for the input matching and a source follower for output matching. Though this LNA is a low power implementation, it provides a relatively low power gain of 10dB and its NF is also as high as 9dB in higher frequency range. Another general approach allowing wideband matching is reported in [2]. The distributed amplifier technique guarantees reasonably good performance in matching and power gain, but occupies more space and consumes high power due to the multiple stages. This paper is addressed to provide a systematic guideline for CMOS LNA design for UWB applications. In this paper, we introduce a practical methodology of CMOS LNA design for UWB applications with respect to impedance matching and noise/power optimizations. The proposed LNA design methodology achieves up to 14dB power gain with the maximum noise figure (NF) of 2dB over 3~5*GHz* frequency range.

II. LNA CIRCUIT SYNTHESIS

In general, it is very difficult to establish a systematic method for LNA design that simultaneously satisfies low NF, impedance matching, and high gain all simultaneously. The major difficulty comes from the fact that the optimal source impedance for best noise performance is normally different from the matching condition for maximum power delivery. So it is very important to confirm initial design decisions of circuit parameters because the noise and impedance matching conditions are highly related to each other. The proposed LNA design is based on a source degenerated topology, which is a widely used for narrowband LNA. The source degenerated topology can maximize power gain by minimizing feedback effect, which mainly sacrifices gain. The synthesized LNA schematic is shown in Figure 1.

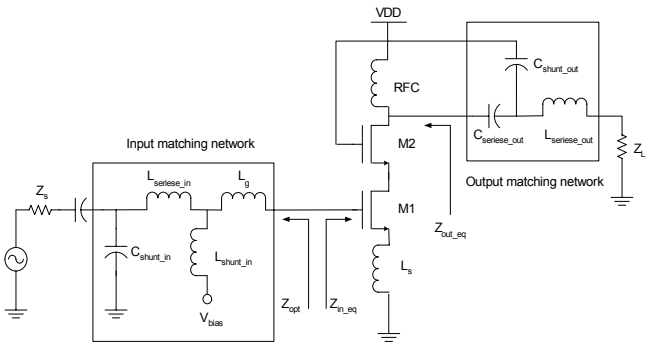


Figure 1. Overall LNA schematic

A. Transistor sizing and bias condition

Since the size of transistor and bias condition determine the power dissipation, it is often recommended to decide them with a certain power budget. However, we should evaluate the size of the transistor versus bias condition carefully, because they are also related to the impedance seen by the input gate. Thus, the first choice is to determine the size and bias condition that satisfies both impedance and noise matching with limited bias current. According to the MOSFET noise analysis [3], the generator (sometimes source) admittance for optimal noise performance is given by (1.1) and (1.2).

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}\left(1-|c|^2\right)} \tag{1.1}$$

$$B_{opt} = -\omega C_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{1.2}$$

where $\alpha = g_m/g_{ds0}$, and noise parameters c, δ, and γ as defined in [3].

For the sake of simplicity, we ignore the correlation of noise so that c can be set to 0. Therefore, we can simplify (1.1) and (1.2) as,

$$R_{opt} \approx \frac{1}{\alpha\omega C_{gs}}\sqrt{\frac{5\gamma}{\delta}} \tag{2.1}$$

$$X_{opt} \approx \frac{1}{\omega C_{gs}} \tag{2.2}$$

Furthermore, by taking into account the degenerative inductor L_s at the source-end, (2.2) can be modified as

$$X_{opt} \approx \frac{1}{\omega C_{gs}} - \omega L_s \tag{2.3}$$

Note the expressions (2.1) to (2.3) represent real and imaginary terms of impedance, unlike (1.1) and (1.2) which are admittance expressions.

It is clear that optimal noise condition and maximum power delivery are obtained simultaneously when $Z_{opt}=Z_{in\_eq}^*$, where Z_{in_eq} is the equivalent input impedance seen by input gate of amplifying transistor given by,

$$Z_{in\_eq} = R_{in\_eq} + jX_{in\_eq} = \frac{g_m L_s}{C_{gs}} + j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right) \tag{3}$$

However, since it is not easy to make both Z_{opt} and $Z_{in\_eq}^*$ equal, thus it better satisfies the inequality as shown in (4) for higher gain. Obviously, smaller resistive term of input impedance seen by the gate-end leads to higher gain.

$$R_{in\_eq} \le R_{opt} \le R_s \tag{4}$$

where R_s is the resistive term of source impedance Z_s.

Since reactance term of Z_{opt} and $Z_{in\_eq}^*$ are almost always matched according to (2.3) and (3), inequality (4) will force Z_{in_eq} to form a bigger circle than Z_{opt} in the Smith chart representation for the frequency range of interest.

As mentioned already, we determine a bias condition with limiting bias current so that DC bias current I_{DS} is a fixed value. For simplicity, we assumed $g_m = \mu_n C_{ox}(W/L)V_{eff}$ and $C_{gs} = (2/3)WLC_{ox}$ by ignoring overlapped channel length L_{ov}, and these give an initial V_{eff} as in (5).

$$V_{eff} \le \frac{2R_s L^2}{3L_s \mu_n} \tag{5}$$

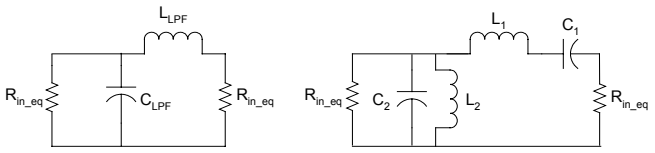
Note that we are considering minimum channel length L in (5). Once we determine the maximum V_{eff}, we can specify the minimum g_m as $g_m \ge 2I_{DS}/V_{eff\_max}$, where V_{eff_max} is the maximum effective voltage.

Assuming $\gamma \approx 2$, $\delta \approx 4$, and $\alpha \approx 5$ because $g_{ds} \approx 0.2g_m$ in active region, (2.1) can be further simplified as $R_{opt} \approx 1/\sqrt{10}\omega C_{gs}$. Thus, we can determine a minimum channel width W as $W \ge 3/2\sqrt{10}\omega R_s L C_{ox}$. Again, minimum channel length is assumed.

B. Input impedance matching

For wideband impedance matching, we have to transfer the source impedance Z_s, which is normally $Z_s = R_s = 50\ \Omega$, to $Z_{in\_eq}^*$ over the frequency range of interest. Conjugate matching will satisfy the optimal noise condition and impedance matching simultaneously as a result of transistor sizing and bias condition described earlier.

First, we derive the 1st order butterworth type bandpass filter from a low pass filter prototype that has been terminated with R_{in_eq} at both the ends, as shown in Figure 2,



$$L_{LPF} = \frac{\sqrt{2}R_{in\_eq}}{\omega_c} \qquad L_1 = rL_{LPF} \qquad C_1 = \frac{1}{\omega_c^2 L_1}$$

$$C_{LPF} = \frac{\sqrt{2}}{R_{in\_eq}\omega_c} \qquad L_2 = \frac{1}{\omega_c^2 C_2} \qquad C_2 = rC_{LPF}$$

Figure 2. Frequency transformation

In Figure 2, ω_c is the center frequency of the target frequency range defined as $\omega_L + (\omega_H - \omega_L)/2 = \omega_L + BW/2$ and BW is the bandwidth required for the target circuit. Note that ω_H and ω_L are the upper and lower stop frequencies respectively. Parameter r is defined by ω_c/BW. Since we are interested in signal reflection and not the 3dB bandwidth, the center frequency is chosen as ω_c, unlike the general bandpass filter development procedure [5], which defines $\omega_c = \sqrt{\omega_H \omega_L}$. The bandpass filter synthesized with the center frequency ω_c has minimum power reflection at the center frequency so that it satisfies the impedance match over the entire target bandwidth at the cost of small gain reduction in the upper frequency range.

Obviously, C_1 and L_1 is equivalent to C_{gs} and L_s+L_g respectively, where L_g is the extra inductor connected to gate. Expressions L_{LPF}, C_1 and L_1 in Figure 2 can determine the choice of L_s as

$$L_s \ge \frac{BW_{\min}}{\sqrt{2}\omega_c^2 g_m} \tag{6}$$

where BW_{min} is the minimum required bandwidth.

By definition, the power loss around the stop band is about 3dB. However, 3dB power loss is unacceptable in

terms of power reflection and hence 50% excessive bandwidth is recommended to guarantee an S11 of –10dB over the frequency band of interest. Since our target frequency band is 3*GHz* to 5*GHz*, we apply 2*GHz* to 6*GHz* bandwidth with the fixed center frequency of 4*GHz*.

Once we design a bandpass filter with R_{in_eq} terminated at both the ends, R_{in_eq} at the input side should be transferred to Z_s with an impedance inverter as shown in Figure 3.

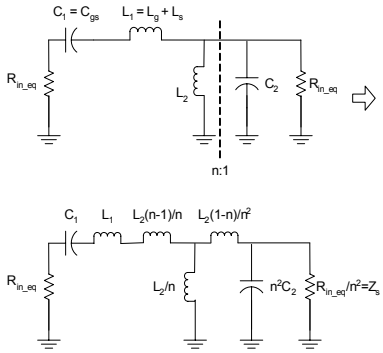


Figure 3. Impedance inverting

Since we addressed R_{in_eq} to be smaller than Z_s, inverting factor n in Figure 3 is less than unity, so that the inductance $L_2(n-1)/n$, which is connected to L_1 in series, is a negative value resulting in a smaller gate inductance L_g. In general, R_{in_eq} is not very small when compared to Z_s, thus n is very close to unity according to the definition $n = \sqrt{R_{in\_eq}/Z_s}$. As a result, the other series inductor, $L_2(1-n)/n^2$, becomes small enough to be implemented either as a simple line in the layout or as a bonding wire.

C. Output impedance matching

Once the input impedance matching is completed, achievable maximum power gain relies on the output impedance matching. A common technique widely used is to employ a source follower following the core amplifier. The Source follower provides an easy output matching method because the output impedance is simply defined by $1/g_{ms}$, where g_{ms} is a gate-source transconductance of the source follower.

However, since the gain of source follower is always less than 0dB, it decreases the overall gain performance, also resulting in a slightly higher NF. Furthermore, the extra amplifier stage without contributing to the gain apparently consumes more power and occupies extra space. Multi-stage amplifier design requires reasonable inter-stage matching that makes the overall design more complicated. For these reasons, a single stage amplifier design providing both input and output impedance matching is more desirable. Better power efficiency can also be achieved using a single-stage amplifier.

In this paper, we introduce two practical output impedance matching methods suitable for wideband LNA design. The first approach is a general matching method similar to the input impedance matching method explained in previous section, while the second is addressed to support mid-range wideband applications such as lower UWB band of 3*GHz* to 5*GHz*. The mid-range wideband matching method relaxes the complexity of the matching network allowing a smaller circuit size.

The equivalent output circuit of the synthesized LNA is a parallel combination of an output resistor r_{ds}, drain-to-source capacitance C_{ds} of the cascode transistor and RFC. The cascode transistor is used to isolate the input and output, and its output resistance r_{ds} controls the overall gain of the LNA.

One interesting fact is that there is a possibility to achieve high gain even with smaller bias current from the relationship $r_{ds} = 1/\lambda I_{DS}$, which implies the larger output impedance with the smaller DC bias current.

In the same manner of the input matching network development, we apply bandpass filter transformation and impedance inverting technique for output matching as shown in Figure 4, which is the first method for general wideband output matching.

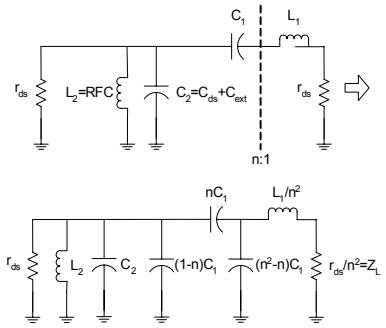


Figure 4. General wideband output matching

The only restriction of the general matching network development is that C_{ds} should be small enough to cancel out the negative capacitance extracted by the impedance inverter represented as $(1-n)C_1$ in Figure 4. Note that n is greater than unity in this case because r_{ds} is much larger than Z_L in most cases. Therefore, the required maximum C_{ds} is derived as

$$C_{ds} \le \frac{2r^2 - n + 1}{\sqrt{2}r\omega_c r_{ds}} \qquad (7)$$

However, the restriction given in (7) cannot be satisfied sometimes due to minimum size requirement to drive enough DC bias current in an amplifying transistor. It is also worth mentioning that the series inductor expressed as L_1/n^2 is considerably small enough to allow the use of a bonding wire as an inductor instead of an integrated inductor.

The second method is addressed to overcome the restriction of the first method, but it is applicable only to mid-range wide bandwidth.

It starts from the assumption that the output impedance of the cascode stage can be approximated to its resistive term, r_{ds}, around a resonant frequency, so that it simply ignores

any reactance terms. Thus, one can build a bandpass filter with r_{ds} terminated at both the ends, and transfer r_{ds} to the load impedance Z_L by impedance inverting technique. However, this method does not achieve wideband matching, because the assumption of output impedance of r_{ds} is valid only around the resonant frequency. To increase the bandwidth, the peak resistive point r_{ds} will have to be mapped to a higher impedance point than Z_L, so that it eventually maps two impedances presented at frequencies in between the center frequency ω_c and the two stop band frequencies, ω_H and ω_L, to Z_L. This method can achieve a wide bandwidth with reasonable impedance matching.

After the bandpass filter and impedance inverter development, new RF choke (RFC) is derived as a parallel connection of the initial load inductor RFC_{init}, selected to give the resonant frequency at the center frequency, ω_c, and the shunt inductor, L_2 of the filter as shown in Figure 5. Note that the parallel combination of RFC_{init} and L_2 synthesizes a smaller RFC resulting in smaller layout area.

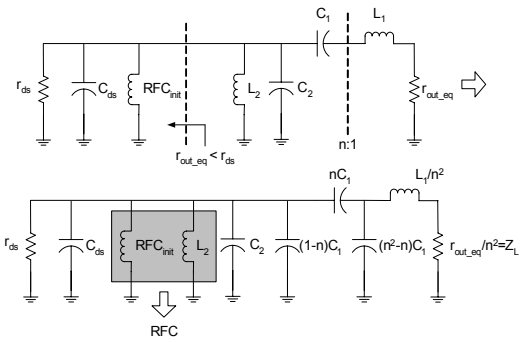


Figure 5. Mid-range wideband output matching

III. Simulation Results

Since FCC allows very low radio emission limit up to –42dBm/*MHz*, UWB applications are very sensitive to noise and require high gain at the receiver side. Also, UWB is intended for low power applications such as wireless sensor networks. The proposed LNA, implemented in TSMC 0.18μm CMOS technology, is ideal for such applications as it consumes only $9mW$ from a $0.9V$ supply. Table 1 summarizes the performance comparison of the proposed LNA with other reported LNA designs targeted for UWB applications.

TABLE I. Performance Comparison

	Tech	S21 (dB)	S11 (dB)	S22 (dB)	BW (GHz)	NF_{max} (dB)	P (mW)
Proposed	**0.18μm CMOS**	**<14**	**<-10**	**<-10**	**3-5**	**2**	**9**
[1]	0.18μm CMOS	<10	<-9.9	<-9.9	2.3-9.2	9	9[1]
[2]	0.18μm CMOS	<8.1	<-8	<-9	0.6-22	6.1	52
[6]	0.18μm SiGe	<21	<-9	<-9	3-10	3	27[1]

[1] Power dissipation on a core amplifier

Post layout simulation results are shown in Figure 6 ~ 8. One can notice that both S11 and S22 are below –10dB and the overall gain is 13.5dB with ±0.5dB flatness. Noise figure is below 2dB over the target bandwidth as shown in Figure 8 and it is a reasonably good noise performance for UWB applications.

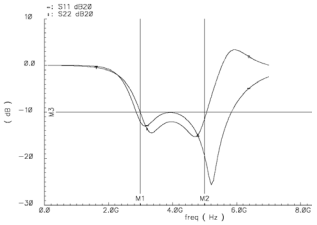


Figure 6. Simulated S11 and S22

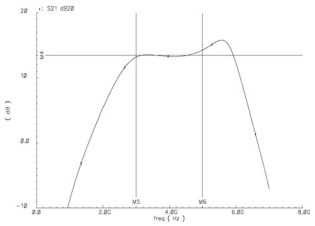


Figure 7. Simulated S21

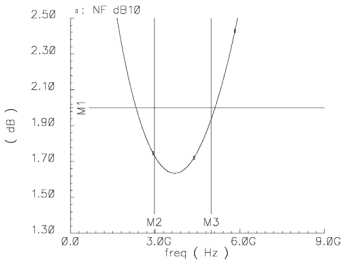


Figure 8. Simulated NF

IV. Conclusion

Based on the theoretical and practical analysis, a systematic procedure for the design of an UWB CMOS LNA is presented. The synthesized LNA guided by the proposed methodology achieves up to 14dB power gain with a suppressed NF as low as 2dB and provides good input and output matching over 3~5GHz. The single stage amplifier consumes only $9mW$ from a $0.9V$ supply, which is distinguished performance improvement achievable with CMOS technology.

Reference

[1] A. Bevilacqua, and A. M Niknejad, "An Ultra-Wideband CMOS LNA for 3.1 to 10.6GHz Wireless Receivers," IEEE International Solid State Circuits Conference, pp.382, 2004.

[2] R. C. Liu et al., "A 0.6-22GHz Broadband CMOS Distributed Amplifier," RFIC Symp. Dig., pp.103-106, 2003.

[3] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[4] J. Goo, et al., "A Noise Optimization Technique for Integrated Low-Noise Amplifiers," IEEE Journal of Solid-State Circuits, vol.37, No.8, August 2002.

[5] L. P. Huelsman, Active and Passive Analog Filter Design – An Introduction, McGraw-Hill, Inc. 1993.

[6] A. Ismail, and A. Abidi, "A 3 to 10GHz LNA Using a Wideband LC-ladder Matching Network," IEEE International Solid State Circuits Conference, pp.384, 2004.