Design of a Tunable Fully Differential GHz Range Gm-C Lowpass Filter in 0.18 µm CMOS for DS-CDMA UWB Transceivers

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***Abstract*—Design of a fully differential sixth order GHz range g_m-C lowpass filter for DS-CDMA UWB (ultra wideband) transceivers is presented. The filter is composed of three identical cascaded biquad sections. The core of the filter is isolated from the source resistance by a folded cascode input stage. An outer negative feedback loop is used to lower the source resistance seen by the core of the filter and extend the bandwidth to a GHz range. Schemes for near orthogonal tuning of bandwidth and passband gain are described and verified. Peaking in the passband is maintained low to avoid distortion and reduced linearity. The proposed lowpass filter is designed in TSMC 0.18 µm CMOS process. Post layout simulations show that the filter bandwidth is tunable over 600 MHz from 800 MHz to 1.4 GHz and the passband gain is tunable over 6 dB, while the passband peaking is maintained below 2 dB. The filter consumes 24.2 mW under supply voltage of 1.8 V.**

Index Terms—**DS-CDMA, UWB, gm-C filter, negative resistance load, lowpass filter**

I. INTRODUCTION

DS-CDMA UWB architecture divides the bandwidth allocated for UWB communications into a lower band that covers the spectrum from 3.1 GHz to 5.15 GHz and an upper from 5.85 GHz to 10.6 GHz. Our transceiver operates in the lower band, and hence the data signal occupies a bandwidth of just over 1 GHz after the down conversion. The lowpass filter has to cover the 1 GHz before the gain is controlled by a variable gain amplifier in both the transmitting and receiving chains. The IIP3 requirement for the transmit chain can be as high as +5 dBm and the IIP3 specification is usually around -8 dBm in the receiver chain. High linearity and large scale integration requires a fully differential architecture to reduce the digital interference and second order distortions due to device mismatch.

Over the years, considerable research has conducted on design of high frequency integrated filters. Direct passive realizations suffer from large area, limited or no tenability, and unreliable simulation models. In addition, the filter parameters are highly sensitive to process variations. Switched capacitor filter implementations are popular owing to excellent tunability, but the switching noise and clock feedthrough degrades the performance of the filter considerably in very high frequency range [1]. Another approach uses op-amps to realize the filter transfer function. In this case, bandwidth of the op-amp should be much larger than the cut-off frequency of the lowpass filter [2]. Therefore, a filter with bandwidth in the GHz range would require op-amps with bandwidth in the range of tens of GHz. Transconductor capacitor (g_m-C) filters are well suited for such a high frequency range, it uses an open-loop (g_m-C) integrator as the basic building block. The g_m-C integrator has excellent gain-bandwidth properties. Two popular approaches exist for g_m-C filter design. In the first approach, a cascade of second order sections (biquads) are used to build a higher order filter, which makes it regular, simple and flexible. The second approach is more complicated. In this approach, elements in a passive realization of the filter transfer function are replaced by their active counter parts resulting in lower sensitivities to component values. Therefore, cascaded biquad based design is highly suitable for very high frequency g_m-C filter design. Only a few architectures have been proposed in literature for gm-C lowpass filters in the GHz range [3] and none of them are fully differential. Traditional method for building biquads is to design a highly linear transconductor and then implement the given transfer function using the transconductor. However, for achieving GHz range bandwidths, the complete biquad should be designed in an integrated manner instead of concentrating on only the transconductor.

The rest of the paper is organized as follows. Section II reviews high frequency g_m-C lowpass biquad filter design. Section III describes the proposed differential biquad structure and the tuning method for varying the bandwidth and the passband gain. Section IV presents the post layout simulation results and section V concludes the paper.

II. PRELIMINARIES

This section reviews the bandwidth limitation due to source resistance in high frequency g_m-C filter design and the design of transconductors for high frequency filters.

2.1 Bandwidth limitation due to source resistance

The typical implementation of a fully differential biquad gm-C lowpass filter is shown in Fig. 1 [2]. This structure is commonly referred to as the "two integrator loop".

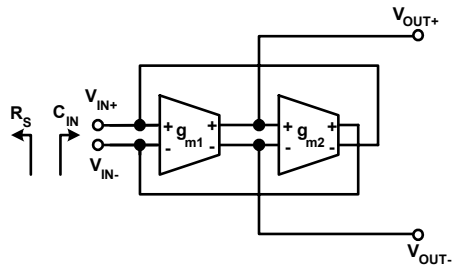

Fig. 1: Biquad Gm-C lowpass filter

For high frequency filters, the impedance at the source of the two integrator loop limits the bandwidth. The source resistance

R_S along with the input capacitance C_{IN} of the two integrator loop leads to a high frequency pole as expressed in (1)

$$\omega_s = \frac{1}{R_s C_{IN}} \quad (1)$$

This pole creates "excess phase" problems which reduce the phase margin of the two integrator loop leading to excessive peaking at the edge of passband or even instability [1]. To minimize this effect, the high frequency pole associated with the source resistance must be at least 10 times larger than the 3-dB cutoff frequency of the lowpass filter. For a filter with bandwidth close to 1 GHz, the pole must be located beyond 10 GHz. Typically the source resistance is 50 ohms for measurement purposes and therefore the node capacitance should be below 300 fF. The input capacitance of the two integrator loop consists of the input capacitance of g_{m1} and the output capacitance of g_{m2}. Consequently, the node capacitance is typically much higher than 300 fF. Therefore novel techniques need to be developed in-order to present a low impedance node at the source of the two integrator loop.

2.2 Transconductor Design

In general, the bandwidth of the transconductors used in the filter must be at least 10 times the filter cut-off frequency [4]. For very high frequency filters, highly linear sophisticated transconductors cannot achieve this large bandwidth and therefore only single element transconductors with no internal nodes can be used.

Output impedance of single element transconductors is quite low and therefore it has to be enhanced. This moves the low frequency pole as close as possible to DC, making it resemble an ideal integrator. One of the popular methods to increase output impedance without introducing unwanted dominant poles is to use a negative resistance load. The idea can be illustrated using the small signal model of a transconductor g_m shown in Fig. 2. The output capacitance is represented by c_o, output resistance by r_0 and the negative load resistance is represented by $-R_L$.

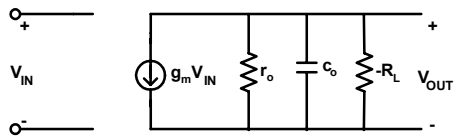

Fig. 2: Small signal model of transconductor with negative resistance load

The overall transfer function is expressed in (2)

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{sc_o + 1/r_o - 1/R_L} \quad (2)$$

From (2) it can be easily observed that a negative resistance load reduces the output conductance of the transconductor. One important side note is that the negative resistance load has to be larger than the transconductor output resistance to ensure that the low frequency pole lies in the left half plane.

III. PROPOSED BIQUAD DESIGN

This section describes the two integrator loop and negative resistance load used in the proposed biquad, overall biquad architecture and tuning schemes for varying the bandwidth and passband gain of the filter.

3.1 Two Integrator loop with Negative resistance load

The two integrator loop used in the proposed biquad filter is shown in Fig. 3. The basic transconductor structure was proposed by krummenacher et al. [5]. This simple modification of adding two devices as source degeneration extends the linear range of the basic transconductor and improves the overall linearity of the biquad filter. One of the drawbacks of this transconductor compared to a simple source coupled differential pair is the mismatch between the current sources that could lead to distortion but the effect can be minimized by a well matched layout.

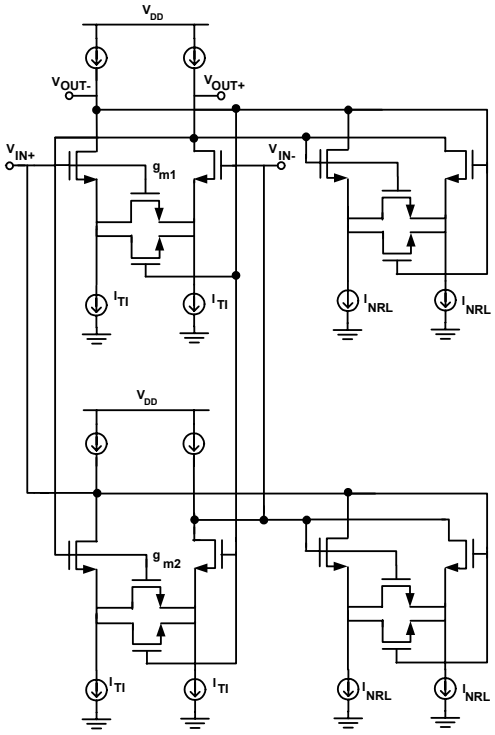

Fig. 3: Two integrator loop with negative resistance load

A number of negative resistance loads have been published in literature based on the principle that a transconductor connected in positive feedback configuration behaves as a negative resistance [6]. The load used in this biquad is also based on the transconductor proposed in [5] in order to improve linearity without increasing complexity.

3.2 Overall Biquad Structure

The complete biquad structure (with the two integrator loop abstracted) is shown in Fig. 4. As mentioned in section 2.1, the core of the lowpass filter should be isolated from the input 50Ω resistance for achieving corner frequencies close to 1 GHz. The proposed biquad uses a modified folded cascode input stage g_{mi}

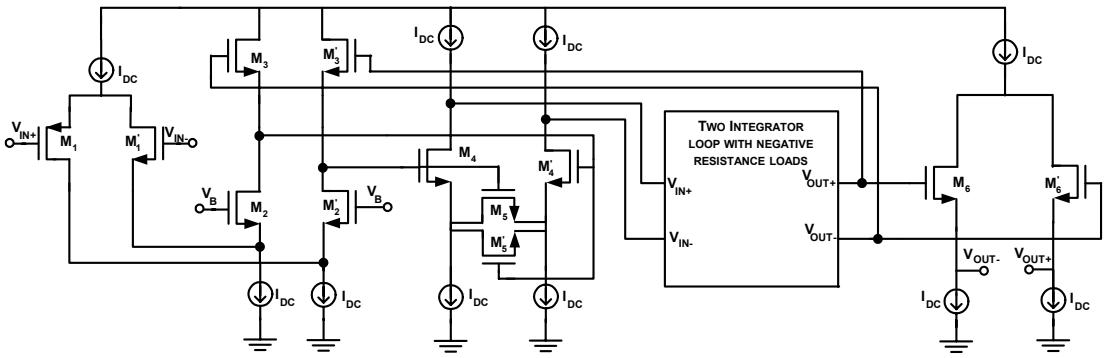

Fig. 4: Overall biquad structure

to isolate the two integrator loop from the source resistance. Folded cascode helps to save head room at the supply voltage of 1.8V and also reduces the Miller effect at the gate of the input pair M_1, M'_1.The load of the cascode stage (M_3 M'_3) and is not cascoded to preserve the voltage head room. Further, the transistor pair M_3 M'_3 looks like a source follower for the output from the two integrator loop. The negative feedback through the load reduces the impedance at the drain of the transistor pair M_2 M'_2. Recall that negative feedback reduces the input impedance by a factor equal to the loop gain. The additional transconductor g_{mb} is required to provide additional gain in the biquad section. It also buffers the lowered source impedance from the large input capacitance of the two integrator loop. The input capacitance of the two integrator loop can be quite large because of cross-coupling and the presence of negative resistance loads. Referring to Fig. 4, the input capacitance of the two-integrator loop consists of the input capacitance of transconductor g_{m1} the output capacitance of transconductor g_{m2} as well the gate and drain capacitances from the negative resistance load. The source follower pair M_6, M'_6 acts as the inter-stage buffer when the biquads are cascaded and also adjusts the common mode level for the input of the succeeding biquad.

3.3 Bandwidth and passband gain tuning

In general, the parameters of a cascaded biquad g_m-C filter are highly sensitive to process variations. The effect is more pronounced in high frequency filters because the node capacitances are of the order of parasitic device capacitances. Therefore electronic tuning of filter parameters is essential to compensate for process variations.

The outer feedback loop in the biquad filter through M_3 M'_3 serves mainly to reduce the source impedance of the two integrator loop. Although, it has some effect on the bandwidth and passband gain of the filter, the effect is not very significant. In order to understand the schemes for tuning bandwidth and passband gain, the outer feedback loop can be ignored without overly modifying the results. Likewise, the finite output conductance of g_{mi} and g_{mb}, are also ignored. Based on these assumptions, a simplified transfer function of the biquad filter structure shown in Fig.4 is expressed in (3).

$$H(s) = \frac{g_{mi}g_{mb}g_{m1}(g_1 + sC_1)}{s^2C_1C_2 + s[C_1g_2 + C_2g_1] + [g_{m1}g_{m2} + g_1g_2]} \quad (3)$$

where $C_{1(2)}$ is the effective output node capacitance and $g_{1(2)}$ is the effective output conductance of the transconductors $g_{m1(2)}$, (including the negative resistance load). The bandwidth of the lowpass filter is expressed in (4)

$$BW = \sqrt{\frac{g_{m1}g_{m2} + g_1g_2}{C_1C_2}} \quad (4)$$

and the passband gain is given in (5)

$$K = \frac{g_{mi}g_{mb}g_{m1}g_1}{g_{m1}g_{m2} + g_1g_2} \quad (5)$$

From (4) we observe that the bandwidth of the lowpass filter mainly depends on the parameters of the two integrator loop. Therefore the bandwidth can be increased by varying the output conductances $g_{1(2)}$ via the bias currents of the negative resistance load I_{NRL}. Conceptually, the negative resistance load increases gain around the cut-off frequency of the filter thereby increasing the bandwidth and introducing peaking at the edge of the passband. The output node capacitances $C_{1(2)}$ are of the order of a few hundred femto Farads and hence the bandwidth varies widely even for small variations in $g_{1(2)}$. From (5), we can conclude that the passband gain is largely unaffected for small variations in $g_{1(2)}$.On the other hand, passband gain of the lowpass filter can be tuned independently by simply adjusting the transconductance g_{mb} via bias current I_B.

IV. POST LAYOUT SIMULATION RESULTS

The complete lowpass filter layout in TSMC 0.18µm CMOS process is shown in Fig. 5.

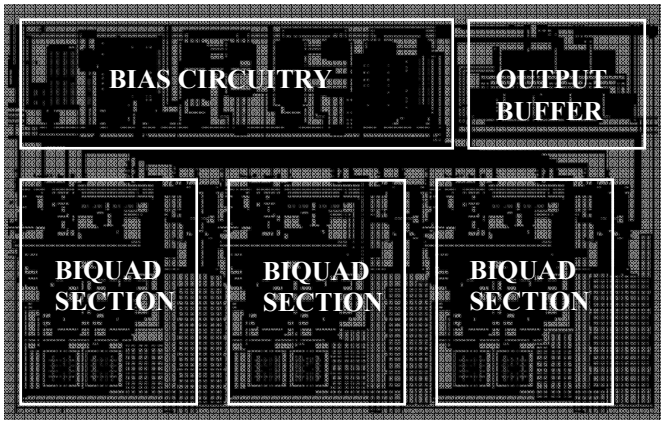

Fig. 5: Layout of the core part of lowpass filter

A sixth order filter with three identical biquads is required to meet the stop band specifications in DS-CDMA UWB transceivers. An output buffer is used to match the output of the lowpass filter to 50Ω differential load impedance. Post-layout simulation results verify the nominal performance in the GHz range and also prove the tuning capability of the lowpass filter. The bandwidth tuning is illustrated in Fig. 6. By adjusting the bias current of the negative resistance load I_{NRL} from 250 µA to 400 µA, the bandwidth can be tuned from 800 MHz to 1.4 GHz. As the bias current increases beyond 450 µA, the bandwidth continues to increase but peaking in the passband exceeds 2 dB.

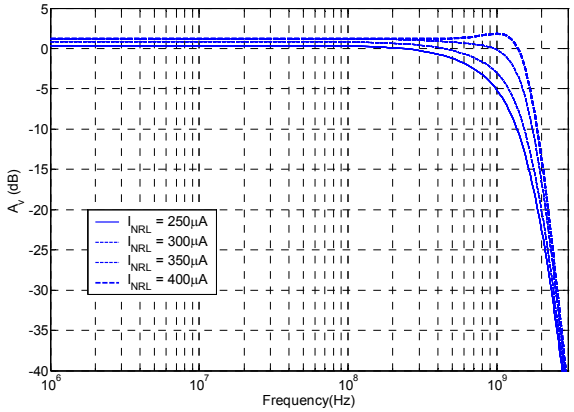

Fig. 6: Bandwidth tuning of the lowpass filter (800 MHz ~ 1.4 GHz)

Passband gain tuning is illustrated in Fig. 7. For this simulation, the bandwidth of the filter is tuned at 1.4 GHz. Passband gain varies from -2 dB to +4 dB for a variation in bias current I_B from 350µA to 550µA . The variation in bandwidth is minimal and the peaking remains below 2 dB.

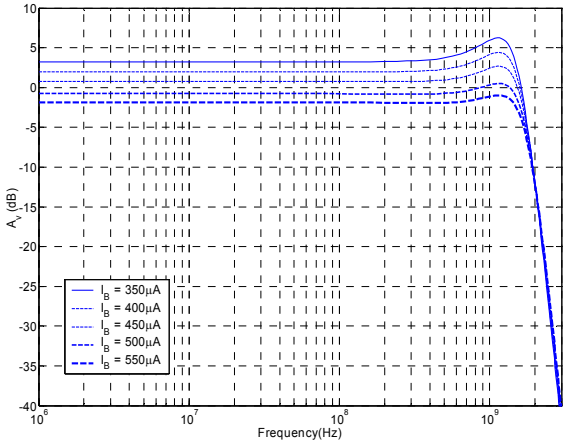

Fig. 7: Passband gain tuning of the lowpass filter (Bandwidth ~ 1.4 GHz)

From the tuning curves, we observe that the passband gain and bandwidth are highly sensitive to the bias current I_B of the transconductor g_{mb} and the negative resistance load I_{NRL} respectively. High sensitivity helps to achieve widely variable bandwidth and passband gain tuning with negligible peaking.

V. Conclusion

A fully differential g_m-C lowpass filter for DS-CDMA UWB transceivers with bandwidth in the GHz range has been designed and simulated. To achieve high frequency operation while maintaining high linearity, simple differential pairs with modified source degeneration are used. Output impedance of transconductors is enhanced by using a linear negative resistance load. The core of the lowpass filter is isolated from the input source resistance by using a folded cascode stage. Source impedance of the two integrator loop is reduced by using negative feedback through the load of the input stage in-order to increase the bandwidth to GHz range. Tuning schemes were developed and verified for nearly orthogonal tuning of bandwidth and passband gain. Table 1 summarizes the performance of the proposed g_m-C lowpass filter. Bandwidth is tunable over 600 MHz (800 MHz ~ 1.4 GHz) and the passband gain is tunable over 6 dB. The filter consumes 24.2 mW from a 1.8 V supply and IIP3 achievable was -4 dBm.

TABLE I: PERFORMANCE SUMMARY

Bandwidth tuning range	800 MHz ~ 1.4 GHz
DC gain tuning range	-2 dB ~ +4 dB
IIP3	-4 dBm
Input impedance	50 Ω (differential)
Output impedance	50 Ω (differential
Technology	0.18 µm CMOS process
Power consumption	24.2 mW

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