11.6 A 3 to 5GHz CMOS UWB LNA with Input Matching using Miller Effect

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Ultra wideband (UWB) radio communication is capable of a high data rate with low radiated power. A key issue for UWB design is LNA input/output matching over a wide bandwidth: 3 to 5GHz for the lower band and 3 to 10GHz for the entire band. Several UWB LNAs have been proposed in recent years. The UWB CMOS LNA presented in [1] employs a Chebyshev filter for input matching and a source follower for output matching. It is intended for low power consumption at the cost of a low power gain of 10dB and a high NF (as high as 9dB at 10GHz). A distributed amplifier scheme for wideband matching is reported in [2]. The scheme, which employs multiple amplifier stages, leads to reasonably good performance in both matching and power gain, but it occupies considerable area and consumes a large amount of power. We propose to exploit the Miller effect for input matching in a CMOS UWB LNA. Our method achieves wideband matching, while requiring only one inductor at the gate in addition to a source degeneration inductor. Our simplified matching network improves the noise figure and reduces the silicon area.

The overall structure of our LNA is shown in Fig. 11.6.1. The input impedance of a source-degenerated MOSFET is often expressed as a series connection of L, C, and R in which the Miller effect is ignored. When the voltage gain from the gate of M_1 to its drain is considered, the Miller effect produces a parallel connection of R and C at the gate of M_1 if the source inductor is absent. This impedance is due to the fact that the voltage gain is dependent on the frequency. However, when a source degeneration inductor is present, such as in our LNA, the equivalent circuit with the Miller effect becomes more complicated, as shown in Fig. 11.6.2. This circuit includes the shunt capacitor C_1, which is also known as the Miller capacitor, and a shunt inductor $L1$ created by the frequency-dependant voltage gain between the gate of $M1$ and the source of $M2$. It is also important to note that an additional capacitor C_2 is present in series with the input. The overall circuit configuration in Fig. 11.6.2 resembles a Chebyshev bandpass filter except for the presence of C_2 and R_1 [3]. However, C_2 is large enough to be ignored at high frequency, and R_1, which is related to the quality factor of L_1, is very small and can be ignored. Therefore, this circuit can be exploited for input matching. The cascode device M_2 improves the reverse isolation, and it also significantly affects the values of L_1 and C_1 in Fig. 11.6.2. Therefore, unlike a typical amplifier design, the bias and sizing of M_2 are highly critical for our LNA design. The load for our LNA is designed to achieve a flat gain over the entire bandwidth of 3 to 5GHz. Normally, the pole at the source of M_2 is much higher than the other poles in this circuit because the driving-point resistance is so small ($1/g_{m2}$). However, when the load impedance at the drain of M_2 is large, the driving-point resistance is bigger than $1/g_{m2}$, so the pole frequency is reduced. The resistance R_L is added to improve the stability by decreasing the quality factor of the LC tank circuit, consisting of L_{L1}, C_{L1}, and C_{L2}. An output source follower is commonly used for 50Ω output matching such as in [1], but we adopt an impedance mapping technique based on our earlier work [4]. Our method saves a source follower and hence reduces the area and the power dissipation. For details, refer to [4].

In general, it is difficult to achieve both noise matching and power matching simultaneously in an LNA design, since the source admittance for minimum noise is usually different from the source admittance for maximum power delivery. However, the Chebyshev bandpass filter configuration exploited in our LNA design as well as in others [2], allows simultaneous noise and power matching. The noise optimal source impedance for a source degenerative topology can be found in [5]. The resistive term seen at the gate of M_1 is designed to be slightly smaller than the resistive term of the noise optimal source impedance to achieve a higher gain by decreasing of the negative feedback (due to the source degeneration). Although the source degeneration provides a smaller resistive term, a 50Ω impedance can be achieved for the overall input matching configuration with the aid of the Miller effect explained earlier. This statement is true since the overall feedback effect increases the resistive term in the input impedance as represented by R_2 in Fig. 11.6.2.

Figure 11.6.3 shows the measured power gain and noise figure of our LNA. The gain remains above 15dB over the frequency range of interest. The overall NF is lower than 2.3dB owing to the simple input matching network and the optimal noise matching. Figure 11.6.4 shows the measured input and output reflection coefficients. S11 is less than -10.5dB over the entire frequency range. The output matching is reasonably good with S22 less than -13.1dB. The two-tone test results for the third-order intermodulation distortion are shown in Fig. 11.6.5. The IIP3 is -9dBm and the input referred 1dB compression point is -23dBm. The proposed LNA core draws 6.4mA from a of 1.2V power supply. Figure 11.6.6 presents a summary of the performance and a comparison with previously published UWB LNAs. The figure shows that the proposed LNA achieves a higher power gain and a lower noise figure than previous circuits, while the power dissipation is comparable. This LNA is fabricated in the TSMC CMOS 0.18μm technology. A micrograph of the presented LNA is shown in Fig. 11.6.7 and its die size is 740μm x 850μm.

Acknowledgements:
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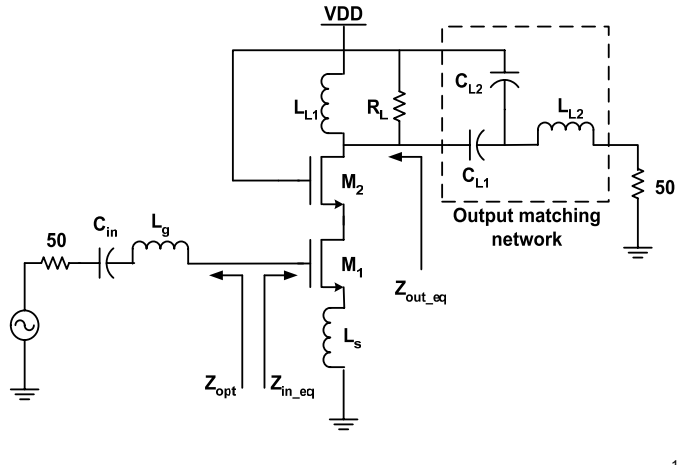


Figure 11.6.1: Overall LNA structure.

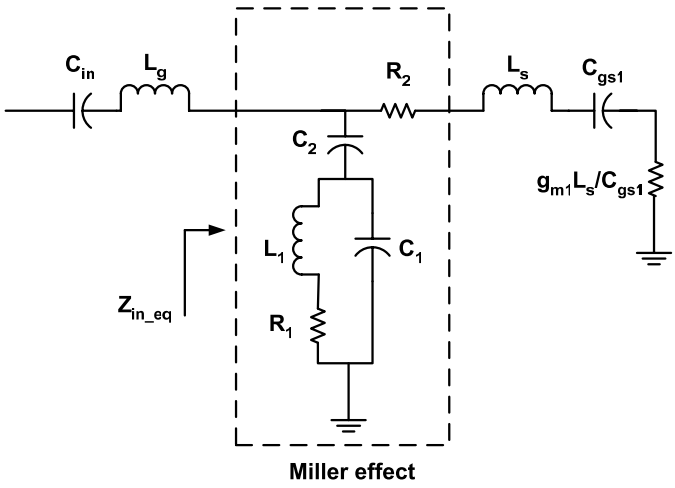


Figure 11.6.2: Equivalent circuit including Miller Effect.

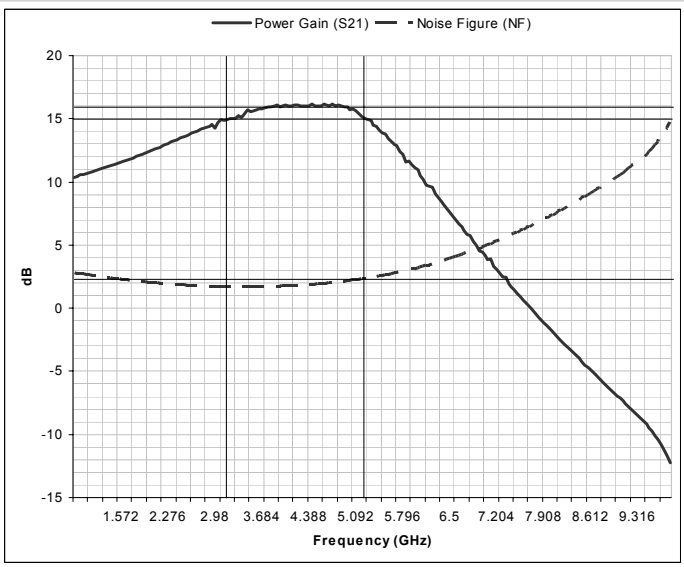


Figure 11.6.3: Power Gain (S21) and Noise Figure (NF).

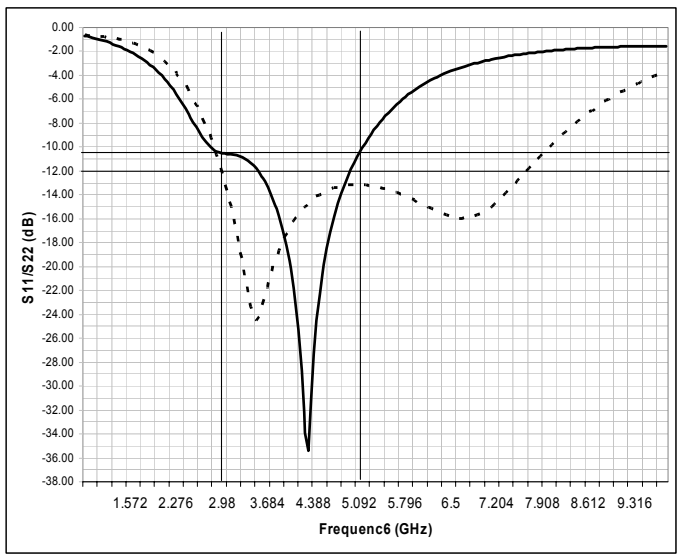
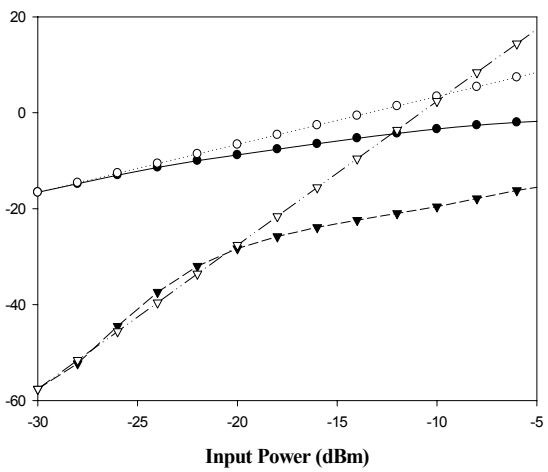


Figure 11.6.4: Input and output matching (S11 and S22).



Input referred P1dB = -23 dBm

Input referred IP3 = -9 dBm

Figure 11.6.5: IIP3 and Input-referred P1dB.

	Tech	S21 (dB)	S11 (dB)	S22 (dB)	BW (GHz)	NF_{max} (dB)	P (mW)
This work	**0.18μm CMOS**	**< 16**	**< -10.5**	**< -13.1**	**3 - 5**[2]	**2.2**	**7.68**
[1]	0.18μm CMOS	< 10	< -9.9	< -9.9	2.3 - 9.2	9	9[1]
[2]	0.18μm CMOS	< 8.1	< -8	< -9	0.6 - 22	6.1	52
[6]	0.18μm SiGe	< 21	< -9	< -9	3 - 10	3	27[1]

[1] Power dissipation in a core amplifier
[2] 1dB bandwidth

Figure 11.6.6: Performance summary and comparison.

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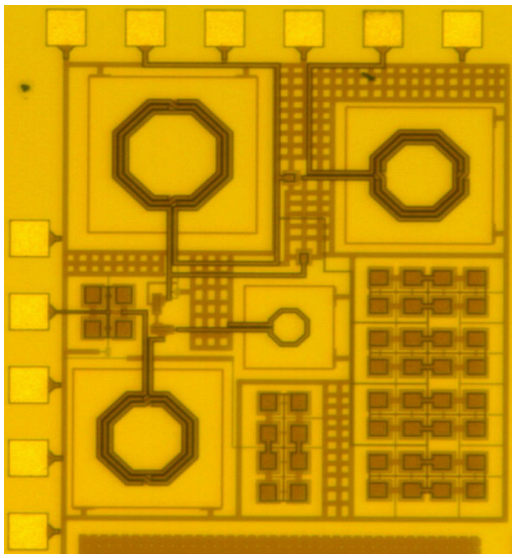

Figure 11.6.7: Micrograph.

