Development and Distribution of TSMC 0.25 μm Standard CMOS Library Cells

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Abstract

Cell-based design is a widely adopted design approach in current ASIC and SOC designs. Standard cell libraries are a collection of basic building blocks that can be used in cell-based designs. The use of standard cell libraries offers shorter design time, induces fewer errors in the design process, and is easier to maintain. This paper presents the TSMC 0.25 μm standard CMOS cell library designed and distributed by the Virginia Tech VLSI for Telecommunications (VTVT) Group, and its impact on the VLSI design community and VLSI education.

1. Introduction

Commercial library cells are proprietary information of the suppliers, and suppliers usually impose certain restrictions on the access and use of their library cells. Those restrictions on commercial library cells hamper VLSI research and teaching activities of academia. In order to address this problem, the Virginia Tech VLSI for Telecommunications (VTVT) group took an initiative to develop and distribute standard cell libraries under the sponsorship of the National Science Foundation. Currently, a TSMC 0.25 μm CMOS standard cell library developed by the VTVT group is available to academia without any restrictions [1], and 258 universities worldwide have received the cell library from the VTVT group as of March, 2007 [2].

2. Design flow

Our cell library was developed using commercial design and simulation tools with the intention to promote users as well as developers to experience the real world design environment. Our standard cell library supports the following tools:

- Synopsys Design Compiler and Design Vision, as library compilation and logic synthesis tools, respectively.
- Synopsys VCS-MX, as a logic simulation tool.
- Cadence SOC Encounter, as a place-and-route tool.
- Cadence Virtuoso, as a verification and layout tool.

In the design flow adopted for our standard cell library, the design entry is a VHDL or Verilog behavioral description. Using Synopsys synthesis and simulation tools, the behavioral description of the design is simulated and then synthesized into a gate-level circuit. The synthesized design is extracted in the Verilog format and imported into the Cadence physical design environment. After place-and-route of the design, the synthesized layout is compared against its schematic.

3. Characteristics

The target technology for our standard cell library is TSMC 0.25 μm CMOS with a supply voltage of 2.5 V. The cells were developed using the NCSU Cadence Design Kit [3] and following MOSIS deep submicron rules. Our cell library contains 84 cells with various primitive gates, multiplexers, and flip-flops with a variety of drive strengths and dummy pads. It includes layout, symbol, schematic views and functional models of all the cells, to support logic simulation and synthesis, place-and-route, and LVS (Logic Versus Schematic). Table 1 and Table 2 include our rules for layout of cells and a sample list of cells from the library, respectively.

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Table 1: Layout Development Rules

Cell Layout Setting	Value
Cell Height	108 λ
Cell Width	Multiple of 9 λ
Metal Pitch	9 λ for metal 1 through metal 4, 18 λ for metal 5
Metal Width	4 λ for all layers
Metal Offset	0 for all layers
Power/Ground Pins/Rails	11λ for VDD and VSS

Note: λ is 0.12 μm.

Table 2: Sample List of VTVT Library Cells

Cell Name	Description
inv_[1,2,4]	Inverter, drive strength 1, 2 or 4
or2_[1,2,4]	2-input OR gate, drive strength 1, 2, or 4
nand4_[1,2,4]	4-input NAND gate, drive strength 1, 2, or 4
xnor2_[1,2]	input XNOR gate, drive strength 1 or 2
mux2_[1,2,4]	2-to-1 multiplexer, drive strength 1, 2, or 4
fulladder	One-bit ripple-carry adder, drive strength 1
ABnorC	(ip1*ip2+ip3)' drive strength 1
cd_16	clock driver, drive strength 16
lrsp_[1, 2, 4]	active D latch with asynchronous low
dp_[1,2,4]	edge triggered D flip

4. Support to VLSI education

About 92 US and 166 international academic institutions have received our cell library for VLSI teaching and research [2]. In addition to development and distribution of our cell library, we have developed and maintained extensive tutorials of CAD tools for VLSI [4]. Major tutorials include: Cadence SOC Encounter, Synopsys Design Vision, and Synopsys VCS Scirocco simulator. A graduate and a senior level VLSI design courses at Virginia Tech use our library cells for class projects. Our online tutorials have also been extensively used in academia and frequently referred by companies. Approximately 20,000 visitors accessed our tutorials since March 2002.

5. Our plan and vision

Since our initial release in 2002, we have received numerous requests to provide more cell libraries. These inquiries forged our group's plan and vision for the next two years. We plan to expand our cell libraries to include TSMC 0.18 μm and 0.13 μm by early 2009. We also plan to develop RAM compilers and data converters (analog-to-digital converters and digital-to-analog converters) for those technologies. We will verify our cell libraries through fabrication of test chips and report the results on our web sites.

As technology advances, it is apparent that our group alone cannot keep up with cell libraries for new technologies. Our long term vision is to adopt the Open Source community approach. Whenever a new processing technology is available through MOSIS, we will provide guidelines (such as cell height, power/ground routing) and ask our users to develop, characterize and deposit a few new cells on our web site. After verification, the cells will be available to the general public, with due credit to contributors. This approach is not only sustainable, but will help the academic community to contribute to VLSI education and research needs and issues.

6. Summary

We believe that our standard cell library has greatly benefited both VLSI design and research communities in academia. Numerous universities across the globe have used our cells and provided feedback regarding future updates. We intend to test and release cutting-edge, reliable and diversified standard cell libraries. Moreover, our major design milestone will be to integrate academic institutions worldwide into a VLSI design community sharing critics and issues regarding pertinent and upcoming design approaches. This project is not only necessary for the present design community; its vision will also significantly impact future designers' performance in industry, as they are being formed in academia through extensive and up-to-date design materials.

Acknowledgment

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References

[1] VTVT web site for a cell library request: www.vtvt.ece.vt.edu/vlsidesign/cell.php
[2] VTVT web site for a users' list: www.vtvt.ece.vt.edu/vlsidesign/users.php
[3] NCSU design kit web site: www.eda.ncsu.edu/wiki/NCSU_EDA_Wiki
[4] VTVT web site for tutorials: www.vtvt.ece.vt.edu/vlsidesign/tutorials.php