On Channel Modeling for Impulse-Based Communications over a Microprocessor's Power Distribution Network

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***Abstract*— As the complexity of a modern microprocessor increases rapidly, the methods of testing/debug take up increasing silicon area and create a cumbersome routing problem. The core Power Distribution Network (PDN) of a microprocessor supplies power to a majority of underlying circuits. In this paper, we propose to explore use of the PDN in a microprocessor as a communication channel for test/debug purposes. Although, there are some common characteristics with Power Line Communications (PLC) over power grid in a residential network, PLC over a PDN is very different in channel characteristics, tolerance to voltage fluctuations and noise characteristics. Further, decoupling capacitors attached to the package and the PDN of a microprocessor makes the PDN a bulky low pass filter. However, it is well known that the parasitic inductance of a decoupling capacitor is more significant beyond the self resonant frequency, and our measurements on an Intel microprocessor indicates that the low pass filter becomes leaky at higher frequencies beyond 1 GHz. In this work, measurements are used to model the PDN of a microprocessor as a communication channel and estimate the path loss characteristics as well as the channel impulse response. Link budget is calculated for the proposed communication system and receiver design considerations are derived. Measurement results and power supply noise analysis indicate that the use of jitter-robust pulse shapes, spread-spectrum techniques and strong coding would be required to communicate reliably over the PDN of a microprocessor.**

Index Terms— **Microprocessor, Power line communication, DFT, Power distribution network**

I. INTRODUCTION

Testing and debug strategies have to be constantly re-invented in order to keep pace with the increasing complexity of a modern microprocessor. Currently, there exists no systematic method to diagnose a system after it crashes and fails to reboot. Also, it is difficult to continuously monitor errors that creep up over a period of time due to variations in temperature and simply aging. To support resilient operations in these constantly varying conditions, extensive monitoring is required throughout the die. Although self-test circuits are used to estimate these variations on a microprocessor die, most of the test circuits are either removed once the chip is deployed on the field or offer very limited access.

The Power Distribution Network (PDN) is ubiquitous across a microprocessor, i.e. a power line is accessible to any internal node. If the power line can be used to communicate with the external world, it can avoid preplanned routing of a data path from a node to an external data pin. This is a highly attractive feature for testing, as the routing of data paths is expensive in design time as well as in silicon area. The ability to monitor internal node values without routing data paths opens up a possibility for fault diagnosis, monitoring transient logic values during built-in self test, sending control data to sensors and for on-line testing. Further, for this application, the target bit rate can be as low as a few hundred bits/sec thereby requiring minimal bandwidth and simple coding schemes.

The use of power lines in an IC environment was introduced by the authors' group in [1] and extended to massive scan-chains in [2]. As noted in [1]-[2], PLC in a microprocessor faces a different set of technical challenges from that of traditional PLC as described below. Most importantly, the noise characteristics of the PDN are different from a traditional PLC. Second, the signal power level in the PDN should be sufficiently small not to disturb the correct operation of the circuit, which makes the recovery of data from a noisy power line difficult. Finally, a microprocessor PDN is heavily decoupled to damp the resonances in the power supply impedance as well as reduce the slew rate of current variations by locally supplying (sinking) currents to (from) the switching nodes. Consequently, the PDN looks like a bulky low pass filter for high frequency signals. However, it is well known that the inductance in the decoupling capacitors becomes significant beyond the self resonant frequency of the capacitors. Also, at microwave frequencies (beyond 1 GHz) the PDN is essentially a distributed circuit and there might be some band of frequencies where the attenuation through the PDN is low [1] – [2]. This band of frequencies can be used for communication over the PDN.

As with any communication system, the first step is the identification of a reliable channel model. Once a channel model is established further work can proceed to select an optimal modulation scheme and explore other aspects like spread-spectrum techniques, coding as well as multiple-access schemes. To explore the feasibility of proposed communication approach, we conducted measurements with a network analyzer on the PDN of an Intel Pentium 4 microprocessor. The impulse response and the frequency selectivity of the microprocessor PDN channel were calculated from the network analyzer measurements.

The rest of the paper is organized as follows. Section II describes the impulse based signaling over a microprocessor PDN, overall architecture of the PDN communications and a basic PDN channel model. Section III describes the setup for channel measurements on an Intel Pentium 4 microprocessor PDN and the measurement results. Section IV reviews the noise sources in the PDN of a microprocessor and also a simplified analytical model for the power supply noise. Section V presents link budget calculations and system design considerations for interference mitigation and co-existence with microprocessor operation. Section VI concludes the paper.

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II. PRELIMINARIES

This section describes impulse based Ultra Wideband (UWB) signaling, overall architecture of the PDN communication approach, and general channel model for the PDN.

2.1 Impulse-based UWB signaling for PDN Communications

Since the Federal Communications Commission (FCC)'s allocation of a UWB spectrum in the range of 3.1 GHz to 10.6 GHz in 2002, UWB has gained phenomenal interest in academia and industry. Compared to traditional narrowband communication systems, UWB signaling has several advantages such as high data rate, low average power, and simple RF circuitry [4]. Shannon's theorem states that the channel capacity C is given as $B \times \log_2 (1+SNR)$ [3], where B is the bandwidth. As the bandwidth B is much larger (on the order of several GHz) for UWB than for a narrowband signal, the SNR can be much smaller for UWB to achieve the same data rate. Therefore, with UWB communications one can often recover data, even if the signal power is close to the noise level. In other words, the power level of UWB signals could be at the noise level of power lines to have little impact to the power integrity.

UWB signaling can be carrier-based or impulse-based, and impulse UWB is more suitable for the proposed application due to its simple hardware [4]. Impulse UWB is based on train of narrow pulses (which are typically a few hundreds picoseconds wide). The most popular pulse shapes used for impulse UWB are Gaussian pulses and their derivatives [4]. In the design of microprocessor PDN and decoupling solutions, the power supply variations are constrained within +/- 5% to maintain data integrity. Say, for a microprocessor with 1.8 V power supply; the amplitude of pulses on the PDN has to be less than 90 mV.

2.2 Overall Architecture

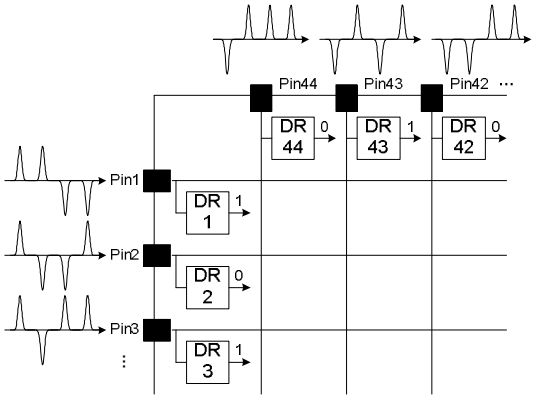

Fig. 1: Overall architecture

The overall architecture of the proposed PDN communications is shown in Figure 1. The impulse modulated data to be sent over the PDN can be applied on any of the power pins. The Data Recovery (DR) blocks are located at the various internal nodes. In addition to sending control data to a single sensor, different data can be sent to different sensors simultaneously using multiple access techniques like Code Division Multiple Access (CDMA) so as to keep the data recovery digital friendly and simple.

2.3 PDN Channel Model

The PDN of a microprocessor with its branched-grid structure behaves as a multipath channel. The impulse response of a general multipath channel can be expressed as in (1).

$$h(t,\rho,\tau) = \sum_{k=0}^{N(t,\rho)} \alpha_k(t,\rho) e^{j\phi_k(t,\rho)} \delta[\tau - \tau_k(t,\rho)] \quad (1)$$

where N (t, ρ) is the number of multipath components received, $\alpha_{k(t,\rho)}$, $\varphi_{k(t,\rho)}$, and $\tau_{k(t,\rho)}$ are respectively, the magnitude, phase and delay associated with a k^{th} multipath component at a given time t and location ρ (two dimensional parameter); and τ is the propagation delay. For an accurate multipath channel model, several measurements taken at different locations are required to characterize the impulse response as well as the delay spread of the different multipath components.

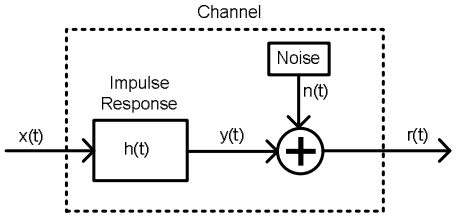

Fig. 2: Typical channel model

A typical channel model is shown in Figure 2. The received signal *r(t)* in this case can be expressed as in (2)

$$r(t) = x(t) * h(t) + n(t) \quad (2)$$

where * represents the convolution operation.

III. CHANNEL MEASUREMENT SETUP AND RESULTS

This section describes the measurement setup for modeling the PDN as a communication channel and the measurement results. The limitations of the measurements are also discussed.

3.1 Measurement Setup

Communication channels can be characterized using frequency domain measurements with a network analyzer and all the time domain parameters like the impulse response and the r.m.s. delay spread can be calculated from the frequency domain measurements [5]. Appropriate fixtures are required to connect the network analyzer to the network to be characterized. These fixtures were not readily available due to the unique nature of our research proposal. Fortunately, we were able to piggy back on a measurement setup typically used for power supply noise measurements and modify it slightly to suit our needs.

The measurement setup is shown in Figure 3. The Pentium 4 processor mounted on a tester board was used for measurement purposes. One port of the network analyzer was connected to a core power supply pin on the tester board and the other port of the network analyzer was connected to a node on the on-chip power distribution network. This setup ensures that the complete microprocessor power distribution network is characterized by the measured S-parameters, including the

power planes in the tester board, package power planes, on-chip power grid and all the different decoupling capacitors.

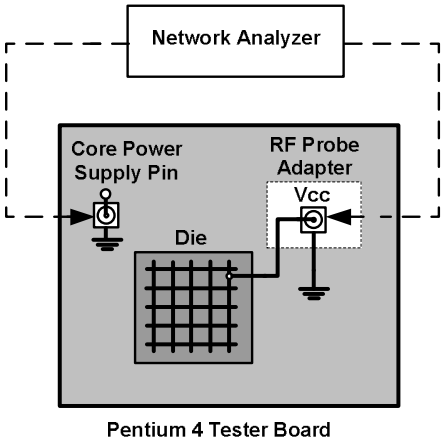

Fig. 3: Measurement setup schematic

A launcher needle used in Time Domain Reflectometer (TDR) measurements to characterize tester board power planes was used to connect one port of the network analyzer to the tester board's core power supply pin. A probing node was created using Focused Ion Bean (FIB) to expose a node on the on-chip power grid. A RF probing adapter connected to the second port of the network analyzer was used to make contact with the exposed node. Since the Pentium 4 die is in a flip-chip package, the probing node created through the back of the die conveniently exposes the lowest metal layer in the on-chip power grid first, thereby characterizing the PDN channel up to a location where the DR block would be located in the final implementation.

The major drawback in this measurement setup is that the die could not be activated. The ports of the network analyzer need to be isolated from DC voltages and bias tees are commonly employed when measurements have to be carried out on circuits requiring an external bias. During full load operation a Pentium 4 die (65 nm version) consumes over 100A from a 1.2V supply. According to the authors' knowledge, the maximum DC current that can be handled by commercially available bias tees is ~ 7A [6]. The huge amount of current drawn poses a similar problem for experts working on power supply noise measurements on an active die.

3.2 Measurement Results

The transmission S-parameter (S_{21}) represents the transfer function of the channel. The path loss of the communication channel is represented by the magnitude of S_{21} and the phase of S_{21} represents the phase response of the channel. The inverse Fourier transform of the complex S_{21} represents the impulse response of the communication channel. The path loss is shown in Figure 4 and the phase response of the PDN channel is shown in Figure 5. The path loss measurements show the existence of narrow sporadic pass bands above 200 MHz. The largest pass band and peak propagation is observed around 2 GHz over a 200 MHz band. As expected, the PDN is quite lossy but the peak observed path loss of ~25 dB is encouraging. The path loss increases above 40 dB beyond 2.5 GHz. The phase of the channel appears mostly linear except for some phase jumps at frequencies 1.3 GHz, 2.6 GHz and 3. 4 GHz. These frequencies correspond to the deep nulls on the path loss characteristics.

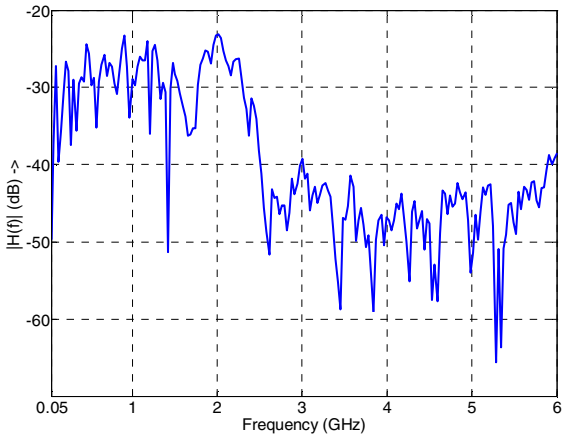

Fig. 4: Measured path loss of the PDN channel

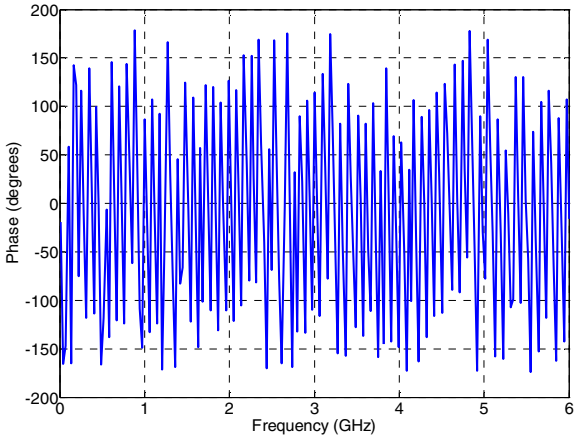

Fig. 5: Measured phase response of the PDN channel

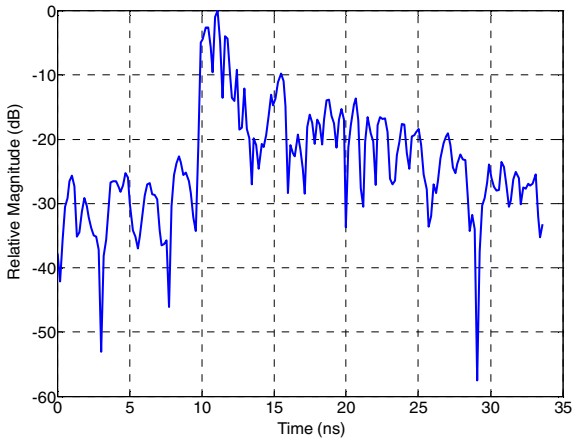

Fig. 6: Low pass impulse response of the PDN channel

The low pass impulse response of the PDN channel is shown in Figure 6. The impulse response has been normalized and plotted in dB scale. The initial delay of ~10 ns is a result of the channel propagation delay. Several multipath components are

observed after the arrival of the original pulse. The time resolution is fixed by the range of frequencies swept by the network analyzer (50 MHz to 6 GHz, in our case) and the number of time samples depends on the number of points used in the calibration (201, in our case). The total period of the impulse response is 33.78 ns (201/ (6-0.05) x 10^{-9}s). An interesting aside is that the second arrival is slightly stronger than the first arrival.

3.3 Limitations of the Measurements

- Only one Pentium 4 part could be obtained with an exposed node on the on-chip PDN. Therefore, the measurement results do not capture spatial variations resulting from multipath effects. Also r.m.s. delay spread of the various multipaths at the receiver could not be estimated.
- Measurements with several Pentium 4 parts are required to characterize the statistical variation in the path loss and pass band locations.
- The microprocessor was not operating during the channel measurements, so the noise resulting from normal operation of the microprocessor should be measured using a separate setup or incorporated into the channel model using an analytical model for the power supply noise.

IV. Power Supply Noise Modeling

This section describes the noise components observed typically in the PDN of a microprocessor and a simplified analytical model for the power supply noise.

4.1 Noise Characteristics in the PDN

Noise in the microprocessor PDN can be broadly classified into three major components as described in [7].

- Cyclostationary background noise resulting from significant amount of switching synchronous to the main clock.
- Strong deterministic components at the frequency corresponding to the main clock and at the frequency of reference clock input to the PLL.
- Low frequency (20 – 100 MHz) noise resulting from resonances in the impedance characteristics of the PDN.

4.2 Noise Modeling

Random power supply noise can only be characterized reliably by multiple measurements and using empirical techniques to capture the statistical variations. The sampled variations measured on the power supply noise of an Itanium processor was reported in [8]. The average variation is less than $20mV_{p-p}$ (with a core supply voltage of 1.05V) but sampled noise voltage is observed over a range of ~ 70mV. Power Spectral Density (PSD) of power supply noise in a high-speed link transceiver was reported in [7]. In this ASIC, apart from the deterministic components, the power supply noise mostly appears white with a PSD of ~-30 dBV/$(Hz)^{(1/2)}$.

Due to the enormous number of noise sources in a microprocessor, one can conclude that the overall noise will tend to a Gaussian process by the central limit theorem. Also, since the majority of switching is periodic with respect to the main clock the noise can be considered to be cyclostationary Gaussian noise. Incidentally, cyclostationary noise models have also been proposed for conventional PLC to characterize synchronous components of the noise in the power line [9].

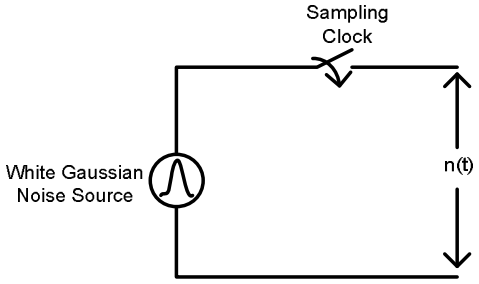

Fig. 7: Simple cyclostationary noise model

Gaussian cyclostationary noise can be modeled simply as shown in Figure 7 by having a white Gaussian noise source model which is sampled periodically [10]. Note that the sampling clock need not be the same as the main clock [7]. However, as previously mentioned, analytical models can only serve as approximations and measurements need to be carried out in order to characterize the time domain dynamics of the noise.

V. System Design Considerations

This section presents the link budget calculations for the proposed communication system and system design considerations for interference mitigation and co-existence.

5.1 Link Budget Calculations

SNR at the input of the DR block can be expressed as in (3)

$$SNR_{DR} = Sig_{IN} - PL_{dB} - N_{floor} \quad (3)$$

where Sig_{IN} is the signal power at the input, PL_{dB} is the path loss through the PDN channel and N_{floor} is the power supply noise floor (all quantities expressed in decibels). Referring back to Figure 4, the path loss for link budget calculations is fixed at 25 dB. Noise Floor is fixed at 20 mV based on the measurements reported in [8]. The calculated SNR values at the input of the data recovery (DR) block for different values of Sig_{IN} are shown in Table I.

TABLE I: Link Budget Calculations for PDN communications

Sig_{IN}		N_{Floor}		Sig_{DR}		SNR_{DR} (dB)
mV	**dBm**	**mV**	**dBm**	**mV**	**dBm**	
100	40.0	20	26.02	5.62	15.00	-11.02
200	46.02	20	26.02	11.24	21.02	-5.0
400	52.04	20	26.02	22.49	27.04	1.02

From the table it can be noted at the amplitude of the pulse at the input needs to be as high as 400mV to get a positive SNR at the output. Although, communication is still possible even if the SNR is negative but that will require a stronger coding scheme in the transmitter and a corresponding increase in the hardware complexity of the DR block.

5.2 Narrow Band Interference Mitigation and Co-existence

Narrrow band interference for the proposed communication approach over a PDN arises from deterministic components located at the main clock and at the PLL reference clock frequencies. The interference to the PDN communication can be mitigated by using spreading. Note that the associated increase in bandwidth is not a major concern in our approach [11]. Spreading also helps to reduce the power spectral density over the information bandwidth and reduces the interference to normal operation of the microprocessor.

VI. CONCLUSION

Feasibility of a communication method over power distribution network of a microprocessor has been studied through channel modeling measurements on the core power distribution network of an Intel Pentium 4 microprocessor. A simplified analytical model could be used to incorporate the noise effects resulting from microprocessor operation. The measurement results and noise analysis show encouraging results for the proposed scheme. We claim that communication over a microprocessor's PDN is feasible without disrupting the normal operation through the use of jitter-robust pulses, strong coding, and spread spectrum techniques.

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