A System-On-Board Approach for Impedance-Based Structural Health Monitoring

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ABSTRACT

Currently, much of the focus in the structural health monitoring community is shifting towards incorporating health monitoring technology into real world structures. Deployment of structural health monitoring systems for permanent damage detection is usually limited by the availability of sensor technology. Previously, we developed the first fully self-contained system that performs impedance-based structural health monitoring. This digital signal processor based system effectively replaces a traditional impedance analyzer and all of the manual analysis usually required for damage determination. The work described here will focus on improving this hardware. Efforts are made to reduce the overall power consumption of the prototype while at the same time improving the overall performance and efficiency. By introducing a new excitation method and implementing a new damage detection scheme, reliance on both analog-to-digital and digital-to-analog conversion are circumvented. These new actuation and sensing techniques, along with the underlying hardware, are described in detail. The reduction of power dissipation and improved performance are documented and compared with both traditional impedance techniques and the previous prototype.

Keywords: structural health monitoring, self-sensing actuator, impedance method, digital signal processor, system-on-board, low-power dissipation

1. INTRODUCTION

The structural health monitoring (SHM) research community is shifting their focus towards incorporating SHM technology into real world structures, and consequently compact hardware with low power dissipation become demanding features for a SHM system. A small form-factor can increase the physical robustness, as well as lower the deployment and maintenance costs, of SHM systems. Low power dissipation makes it possible to use power harvesting units exploiting ambient vibration and temperature gradients, which contributes to cost reduction.

Previously, we have developed the first fully self-contained prototype that performs impedance-based SHM, which consists of a digital signal processor (DSP) evaluation module (EVM), an analog-to-digital converter (ADC) EVM, and a digital-to-analog converter (DAC) EVM [1,2]. This DSP based multi-board system effectively replaced a traditional impedance analyzer and manual analysis required for damage assessment. The procedures of structural excitation, data acquisition, and damage assessment are performed in a matter of seconds, and damage in a structure can be detected almost instantaneously. However, as this prototype is implemented on three evaluation boards, it has limitation on practical deployment due to high power dissipation and a large form factor. There has been an effort to develop a compact hardware for SHM and sensor diagnostics utilizing an impedance converter / network analyzer integrated circuit (IC) AD5933 from Analog Devices [4]. Though a SHM system with a custom printed circuit board (PCB) which is capable of acquiring impedance measurements and wirelessly transmitting the raw data was developed, it must still rely on a separate computer for damage assessment.

We have proposed a new algorithm, digital low-power SHM, that performs SHM operations with binary signaling [3] to reduce computational complexity, simplify hardware implementation, and accordingly lower the power dissipation. This digital low-power SHM algorithm completely eliminates the reliance on analog signaling for structural excitation, and,

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Sensors and Smart Structures Technologies for Civil, Mechanical, and Aerospace Systems 2007,
edited by Masayoshi Tomizuka, Chung-Bang Yun, Victor Giurgiutiu, Proc. of SPIE Vol. 6529,
65290O, (2007) · 0277-786X/07/$18 · doi: 10.1117/12.715791

consequently, data acquisition can also be performed using a binary format. Therefore, implementing a SHM system without incorporating an ADC or a DAC to achieve compact hardware development with lower power dissipation became possible.

In this paper, we present prototype development for the digital low-power SHM algorithm utilizing binary signaling in detail. The binary signaling algorithm is briefly described and compared with the previously utilized analog based algorithm. By using a set of test structures, the functionality is verified and the performance, in terms of damage detection and power dissipation, is evaluated. The prototype demonstrates the feasibility of implementing a SHM system on a single PCB.

2. OPERATION AND ARCHITECTURE

Impedance-based SHM performs three major operations: excitation signal generation, sensor actuation and sensing, and damage assessment. An excitation signal can be generated by a traditional function generator or by a DSP. The excitation signal generated by a DSP is transmitted to a self-sensing actuator bonded to the structure. A self-sensing actuator, which is made from piezoelectric materials, generally utilizes MFC (Micro-Fiber Composite) or PZT (Lead Zirconate Titanate) patches. A PZT patch is adopted for our prototype. Once the excitation signal from the DSP reaches the self-sensing actuator, the structural response induces stress on the actuator to produce a response signal, which is altered from the excitation signal according to the structure's mechanical impedance. The response signal can be sensed by a traditional impedance analyzer or by a DSP. The recorded structural response is post-processed to create a signature and calculate a damage metric, either in a computer using a general purpose computing software such as MATLAB, or in a DSP. A signature is a frequency domain representation of the structural response that varies depending on the structure's mechanical impedance, and the first signature, called a baseline, is stored as a reference under the assumption that the structure is initially in a healthy condition. The structural response is measured a certain number of times, and their average generates an impedance signature. The damage metric, a difference between the baseline and the current signature, is compared to a preset threshold value to determine if the structure has been damaged. Since our ultimate goal is to develop an SHM system on a single board, we have proposed to use a DSP as an excitation signal generator, structural response sensor, and a post-processor to effectively eliminate once necessary equipment such as a function generator, an impedance analyzer, and a computer out of the SHM system [1-3].

In developing our first prototype described in detail in [1,2], we have used a sinc waveform to excite the structure, which is an impulse-like signal containing multiple frequency components from DC to very high frequency depending on the sampling speed of the ADC. The sinc waveform is generated by a DSP and sent out through a DAC to the PZT bonded to the structure. The structural response is then measured through an ADC to provide an estimated voltage level to the DSP. Finally, the DSP performs a fast Fourier transform (FFT) on the received voltage sequence to create the baseline or a signature, and calculates the root mean squared deviation (RMSD) damage metric between the baseline and a current signature.

The digital low-power SHM algorithm proposed in [3] is applied to this system-on-board approach prototype development, and the overall architecture is shown in Figure 1. Instead of the sinc waveform used in our previous prototype, digital rectangular pulse trains of various frequencies, generated by the pulse width modulation (PWM) signal generator of the DSP, are proposed to excite the structure. Since the excitation signal is a binary sequence, the reliance on a DAC is circumvented. Structural response through the PZT is also sensed with only the sign (positive or negative) of the voltage rather than multiple voltage levels, and this change results in the elimination of ADC use.

As illustrated in Figure 1, there are two signal paths in performing sensor actuation and sensing: a reference signal path and a measuring signal path. The reference signal path is a route through which the excitation signal from the PWM is directly fed back into the DSP, and the measuring signal path is the actual excitation and sensing signal path through an Opamp and a comparator. Both signal paths are going into general purpose input output (GPIO) pins of the DSP for comparison. Variations between the two signals are mainly caused by the mechanical impedance of the structure. These differences can be represented in terms of a variation count by counting the number of differences between the received reference path sequence and measuring path sequence at each frequency component. An ensemble average of a certain number of variation counts produces a signature. Finally, the damage metric is calculated as a sum of absolute differences between the baseline and a signature through the frequency components and is compared with the preset threshold value to determine whether the structure is damaged.

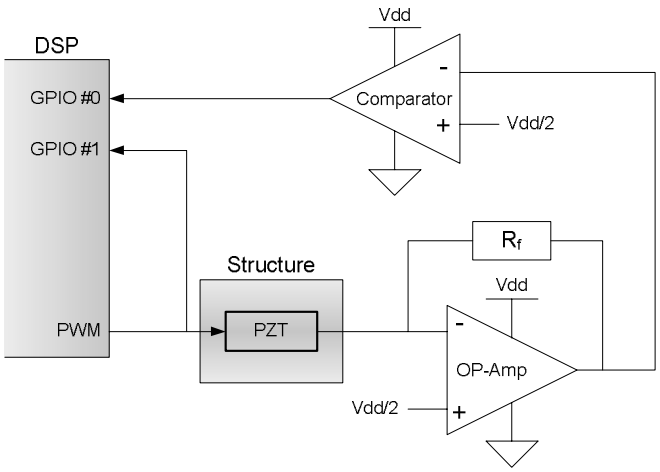

Figure 1 Overall Architecture

3. IMPLEMENTATION

3.1 Hardware Characteristics

Our prototype implementing digital low-power SHM is based on the TMS320F2812 EVM from Texas Instruments [5]. TMS320F2812 is a 32-bit fixed point DSP supporting up to 150 million instructions per second (MIPS) operation. The maximum core operating clock frequency is 150 MHz and can be reduced down to 15 MHz by changing the phase locked loop (PLL) multiplier setting. The peripheral clock frequency can be selected as high as the core operating clock frequency or as low as the core operating clock frequency divided by 14. The supply voltage for the DSP core is 1.8 V at 130 MHz and 1.9 V at 150 MHz. For Input/Output utilization, the supply voltage is 3.3 V, while the recommended supply voltage for the entire EVM is 5 V. Our digital low-power algorithm relies on binary signaling rather than multiple voltage levels for structural excitation, requires simple accumulation instead of FFT operations which involves intensive multiplications for signature generation, and takes advantage of subtraction instead of a square root operation for damage metric calculations. Hence, we can employ a low-power, relatively slow 32-bit fixed point DSP, while the previous sinc waveform based prototype required a power-hungry 225 MHz 64-bit floating point DSP.

In addition to the DSP, there are two more IC devices involved for PZT excitation and sensing operation. The excitation and sensing operation requires two buffers, a comparator, and an Opamp. A four-channel Opamp OPA4342 from Texas Instruments is employed to implement two buffers and a comparator, and a single-channel Opamp TLV2770 from Texas Instruments is adopted for the Opamp [6-7]. Some miscellaneous components, such as resistors and an LED, are also included.

One buffer is connected between the digital output from the DSP and the PZT on the measuring path, and the other buffer is connected between the digital output from the DSP and the digital input to the DSP on the reference path to avoid loading effects. If a buffer is not inserted between two components on a signal path, a voltage drop occurs due to the voltage dividing between the output impedance of the component transmitting the signal and the input impedance of the component receiving the signal. Thus, a buffer, whose ideal input impedance is infinite and ideal output impedance is zero, is inserted between them to ensure maximum voltage transfer. A comparator is connected to the output of the Opamp to convert the structural response into a digital signal to be measured by the DSP. This comparator performs the function of a buffer as well. In the previous prototype, we did not have to insert buffers because the DAC EVM and ADC EVM had buffers on-board. For this digital method prototype, we effectively replace high-power consuming DAC EVM and ADC EVM with a buffer and a comparator, which resultantly reduces power dissipation significantly and miniaturizes the form factor.

The prototype is shown in Figure 2. TMS320F2812 EVM is 7.62 cm X 12.7 cm, and the external bread board consists of Opamp ICs, resistors and an LED. The LED is turned on and off to indicate structural damage based on the detection result calculated by the DSP.

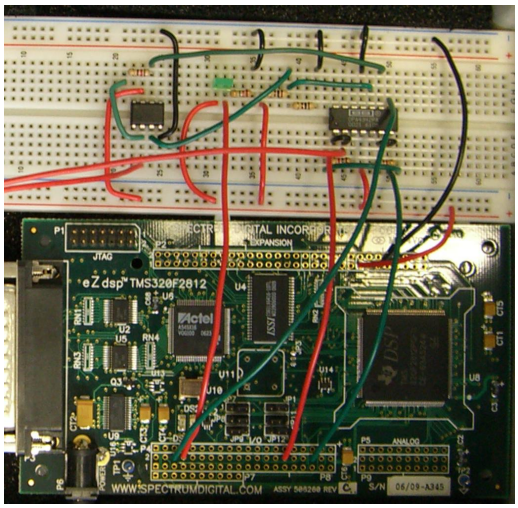

Figure 2 Prototype using TMS320F2812 EVM

3.2 Test Structure and Detection Frequency Range

To verify the functionality and evaluate the performance of the prototype, we composed a test structure as shown in Figure 3. The test structure consists of three aluminum beams of the same dimension but in different mechanical damage states. The exact dimensions of three beams and their damage are illustrated in Figure 4. The first beam without a hole represents a healthy reference condition, and the other two beams with a hole in the middle demonstrate damage on the structure. These three beams are connected to a rotary switch, so by rotating the switch a structure with a different mechanical condition can be selected. As opposed to removable damage, such as tightening and loosening bolts or applying magnets, a structure with permanent damage that can be chosen using a switch provides us the exact same mechanical characteristics of healthy or damaged structural conditions throughout the test.

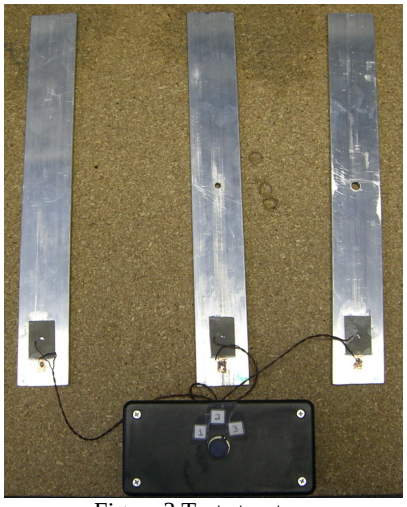
Figure 3 Test structure

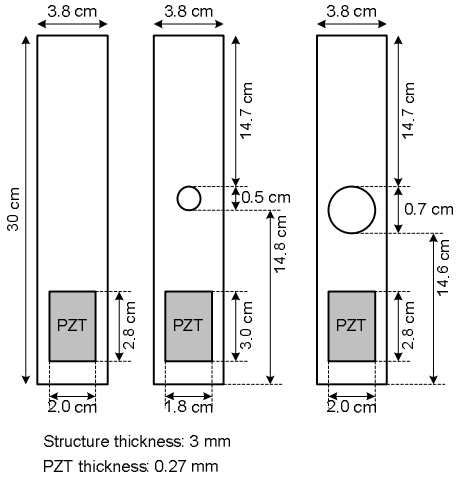

Figure 4 Test structure dimension (not in scale)

Since the DSP utilized in our prototype has limited data memory size, it is efficient to focus on a frequency range sensitive to the structural excitation. Impedance analysis is performed on the PZT bonded to the test structure using a HP 4194A impedance analyzer to determine the detection frequency range. The impedance measurement frequency range is from 100 Hz to 100 KHz with a frequency step size of 10 Hz. To alleviate noise effects, 35 measurements were taken, and the maximally occurring value was selected at each frequency through a histogram analysis. Values of resistance and reactance, the real and imaginary parts of the measured impedance, at three different structural conditions are shown in Figure 5 and Figure 6, respectively. After analysis, it is observed that the frequency range from 12 KHz to

25 KHz is highly sensitive to excitation, and different damage characteristics alter the impedance at certain frequencies by arbitrary amounts. Therefore, based on this measured impedance, the detection frequency range for the prototype is selected as 12 KHz to 25 KHz.

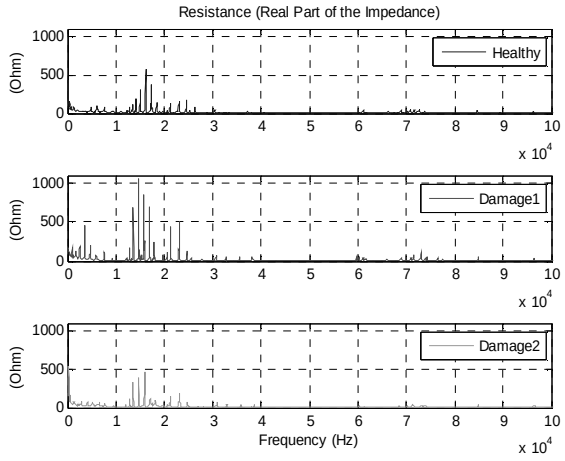

Figure 5 Resistance (real part of the impedance)

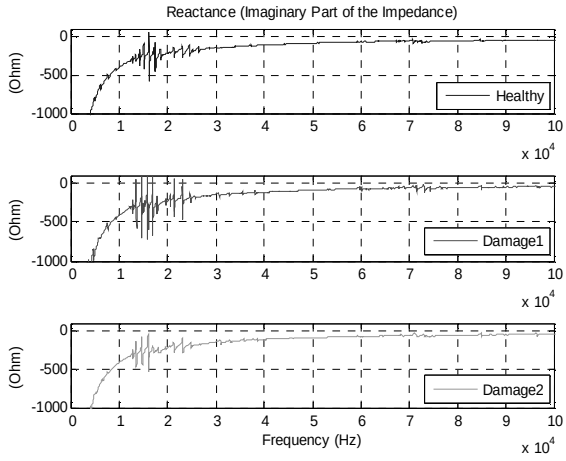

Figure 6 Reactance (imaginary part of the impedance)

3.3 Frequency Resolution

The frequency resolution in the detection frequency range mainly depends on the available data memory size and the peripheral clock frequency. Memory allowance for user data in TMS320F2812 is 960 × 16-bit. Since a signature is an ensemble average of certain number of variation counts, a certain number of consecutive variation counts at each frequency component should be stored in the memory. The baseline, current signature, and the difference between them also have to be stored for a damage metric calculation. Thus, the required memory space N_{mem} is

$$N_{mem} = (3 + N_{avg}) \times N_{freq} \tag{1}$$

where N_{avg} is the number of variation counts per signature and N_{freq} is the number of frequency components per variation count. Setting N_{avg} as eight, we obtain the maximum number of frequency components per variation count $N_{freq,MAX}$ as 87 from the following relationship.

$$N_{freq,MAX} = \left\lfloor \frac{960}{(3+8)} \right\rfloor = 87 \tag{2}$$

The excitation frequency is controlled by changing the pulse width of the PWM output, and the pulse width is managed by decrementing the number of peripheral clock cycles per pulse. For example, when the default clock configuration is used, the peripheral clock frequency is 75 MHz. As the pulse width of the lowest frequency component 12 KHz is 83 μsec and that for the highest frequency component 25 KHz is 40 μsec, the number of peripheral clock cycles per pulse width is 6250 and 3000, respectively. To minimize the computational complexity of calculating the pulse width for each frequency component, the number of peripheral cycles per pulse width is decremented by a constant amount, instead of calculating decrement cycles to generate linearly increasing excitation frequency. As the maximum number of frequency components per variation count calculated based on the memory allowance is 87 from equation (2), the minimum decrement of pulse width, in terms of the number of peripheral clock cycles $N_{pclk,MIN}$, is

$$N_{pclk,MIN} = \left\lceil \frac{(N_{pclk,low} - N_{pclk,high})}{N_{freq,MAX}} \right\rceil = \left\lceil \frac{(6250 - 3000)}{87} \right\rceil = 38 \tag{3}$$

where $N_{pclk,low}$ and $N_{pclk,high}$ are the number of peripheral clock cycles for the lowest detection frequency and the highest detection frequency. $N_{pclk,low}$ and $N_{pclk,high}$ are 6250 and 3000, respectively, in this example.

Figure 7 shows the number of peripheral clock cycles versus calculated excitation frequency and the frequency resolution at each excitation frequency component. Since the number of peripheral clock cycles is decremented linearly, the excitation frequency does not linearly increase. The frequency resolution increases as the excitation frequency increases instead of providing a constant frequency resolution within the detection frequency range. The average frequency resolution through the excitation frequency range is 151 Hz, in this example.

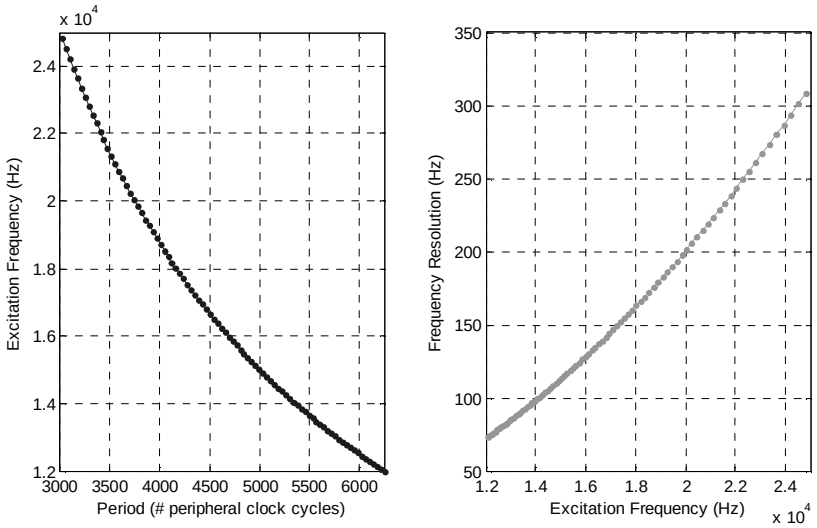

Figure 7 Example calculated excitation frequencies and frequency resolution – Peripheral clock frequency is 75 MHz and the number of frequency components in the detection frequency range is 87.

4. PERFORMANCE ANALYSIS

4.1 Damage Detection

To prove the damage detection capability of the presented digital low-power prototype, measurements have been preformed with varying core operating clock frequencies and peripheral clock frequencies. As a reference performance for verification purposes, RMSD values are calculated from the measured impedance shown in Figure 5. The real part of the impedance is used as it reflects the structural damage more clearly than imaginary part of the impedance [8]. The calculated RMSD value for Damage 1, which is the middle beam with a smaller hole in Figure 3, is 98.16, and that for Damage 2, which is the first from the right with a larger hole, is 64.59. Therefore, we are expected to observe larger damage metric from Damage 1 than from Damage 2, as well as larger damage metric from damaged structure than from the healthy structure.

For this experiment, the number of samples, equivalent to four periods of the excitation signal with the lowest detection frequency, is output through the PWM. The time period of each excitation frequency remains the same to excite the structure with the same amount of the energy for each frequency component. Table 1 summarizes the damage metric with different core operating clock frequencies and peripheral clock frequencies. The peripheral clock frequency was kept as the default value. For each metric shown, the damage metric was measured ten times, and the average of the ten calculations is displayed. Comparing the damage metric of the damaged structures to that of healthy structure, we can observe that the peripheral clock frequencies from 75 MHz to 7.5 MHz can detect damage as expected in accordance with the RMSD values calculated from the measured impedance. Also noticeable is the minimum core operating clock frequency of 15 MHz can fully support all operations for excitation signal generation and damage assessment.

Table 1 Core operating clock frequency and damage detection performance

Core Operating Clock	Peripheral Clock	Damage Metric		
(MHz)	(MHz)	Healthy	Damage 1	Damage 2
150	75	584	173554	144597
105	52.5	513	120924	101322
60	30	430	68879	58325
15	7.5	311	20267	13044

Since it was shown that the slowest operating clock frequency can support the digital low-power algorithm, another experiment was performed at the slowest operating clock frequency while varying the peripheral clock frequency. Table 2 shows the damage metric comparison with lower peripheral clock frequencies at a 15 MHz core operating clock frequency. The number of frequency components and pulse width decrement are calculated based on equation (1) and equation (3), and the average frequency resolution is consequently determined. Clearly, the peripheral clock frequency of 1.25 MHz still can detect damage, and only 55 frequency components in the 12 KHz to 25 KHz detection frequency range, with an average frequency resolution of 240 Hz, are sufficient for damage detection.

Table 2 Peripheral clock frequency and damage detection performance

Core Operating Clock	Peripheral Clock	Damage Metric			# Frequency Components	Pulse Width Decrement	Average Frequency Resolution
(MHz)	(MHz)	Healthy	Damage 1	Damage 2		(# Peripheral Clock Cycles)	(Hz)
15	3.75	108	7172	4982	82	2	159
15	2.5	73	3403	2753	55	2	240
15	1.875	85	3724	2759	82	1	160
15	1.5	76	2221	1925	66	1	200
15	1.25	61	1755	1400	55	1	240

4.2 Power Dissipation

Power dissipation with different core operating clock frequencies is compared as shown in Table 3. The power dissipation was calculated based on the measured current dissipation and the EVM supply voltage. When the core operating clock frequency is 150 MHz, the power dissipation is ranged from 1.7 W to 1.8 W depending on the structural condition. When there is damage on the structure, the indication LED is turned on, and the power dissipation increases by 105 mW. It is noticeable that the whole SHM system can operate under 1 W with a core operating clock frequency of 15 MHz, regardless of the existence of damage on the structure. Even when the LED is on, the power dissipation is only 900 mW. The total power dissipation will be further reduced when we enclose the miscellaneous external circuitry on to a single PCB and utilize miniaturized components, such as surface mount resistors and LEDs as well as small outline packaging for Opamp ICs. In our previous prototype, it was observed that the power dissipation increase by turning on a surface mount LED was insignificant.

Table 3 Core operating clock frequency and power dissipation

Core Operating Clock	Supply Voltage	Current Consumption		Power Consumption	
(MHz)	(V)	(mA)		(mW)	
		LED Off	LED On	LED Off	LED On
15	5	158	180	790	900
60	5	222	243	1110	1215
105	5	285	306	1425	1530
150	5	343	364	1715	1820

The power dissipation of our previous prototype using sinc excitation implemented on multiple evaluation boards is compared with that of the presented digital low-power prototype. For a fair comparison, the power dissipated for excitation signal generation, sensor actuation and sensing, and damage assessment are compared. The previous prototype incorporates a DSP EVM, a DAC EVM and an ADC EVM, while the presented prototype involves a DSP EVM with miscellaneous supporting circuitry. As summarized in Table 4, the previous prototype consumes total 4.01 W. Under an assumption that the structure remains in healthy status most of the time, the typical power dissipation of the presented prototype is 790 mW, which is only 20 % of the total power dissipation of the previous prototype. By adapting the digital low-power SHM algorithm, the power dissipation from the ADC and DAC has been completely eliminated, and the simple algorithm made it possible to use a lower performance DSP to decrease the power dissipation from the DSP itself.

Table 4 Power dissipation comparison

Component	Power Dissipation (W)	
	Previous Sinc Excitation	Presented Digital Excitation
DSP	1.58	0.79
DAC	0.75	N/A
ADC	1.68	N/A
Total	4.01	0.79

5. CONCLUSION

We have presented the implementation of a self-contained digital low-power SHM system using a DSP EVM. The digital low-power algorithm capitalizes on a digital rectangular pulse train for structural excitation and measures the structural response in a digital format to eliminate the use of both a DAC and ADC. The DAC is effectively replaced by a buffer, and a comparator substitutes the ADC. The typical power dissipation is 790 mW, which is only 20 % of the power dissipation of our previous prototype. The 80 % reduction on the power dissipation is obtained by developing the SHM system on one board with miscellaneous external circuitry eliminating DAC and ADC. Another factor reducing the power dissipation is the relaxed core operating clock frequency achieved by simplifying the excitation signal generation and damage assessment operation. Measurement results obtained using the test structure proved that the developed SHM prototype provides reliable performance. This prototype utilizing digital low-power SHM algorithm successfully demonstrated the feasibility of system-on-board implementation of the SHM system.

ACKNOWLEDGEMENT

This material is based upon work supported by the National Science Foundation under Grant No. 0426777. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the National Science Foundation.

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