

Development of TSMC 0.25 μ m Standard Cell Library

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Abstract

Standard library cells are basic building blocks for ASIC (Application-Specific Integrated Circuit) design, which improves designers' productivity through reduced design time and debugging. In this paper, we present the development of a CMOS standard cell library by the VTVT (Virginia Tech for VLSI and Telecommunications) Lab.

Keywords: VLSI design, CAD tools, Standard cell library.

1. Introduction

Commercial library cells are companies' proprietary information, and understandably, companies usually impose certain restrictions on the access and use of their library cells. Those restrictions on commercial library cells severely hamper VLSI research and teaching activities of academia. To address the problem, the VTVT (Virginia Tech for VLSI and Telecommunications) Lab of Virginia Tech has developed a TSMC 0.25 μ m CMOS standard cell library under the sponsorship of the National Science Foundation and distributed it to over 258 universities worldwide [1].

2. Features of VTVT's Standard Cell Library

The VTVT's cell library intends to support a cell-based VLSI design flow starting from a behavioral description to a layout. Specifically, it supports major tasks such as logic simulation and synthesis, place and routing (P&R), and layout versus schematic (LVS). The VTVT's cell library has been targeted and tested with Synopsys tools for logic simulation and synthesis, and with Cadence tools for P&R and physical design. It has 84 cells including both combinational and sequential cells with different drive strengths. Some of the representative cells are listed in Table 1.

Figure 1 through Figure 3 show cell views of 2-input AND gates with different driving strengths.

Table 1: List of VTVT's Representative Library Cells

Cell Name	Description
buf_[1,2,4]	Non-inverting buffer, drive strength 1, 2, or 4
inv_[1,2,4]	Inverter, drive strength 1, 2 or 4
and3_[1,2,4]	3-input AND gate, drive strength 1, 2, or 4
or2_[1,2,4]	2-input OR gate, drive strength 1, 2, or 4
nand4_[1,2,4]	4-input NAND gate, drive strength 1, 2, or 4
nor2_[1,2,4] 2	input NOR gate, drive strength 1, 2, or 4
xor2_[1,2] 2	input XOR gate, drive strength 1 or 2
xnor2_[1,2] 2	input XNOR gate, drive strength 1 or 2
mux2_[1,2,4]	2-to-1 multiplexer, drive strength 1, 2, or 4
fulladder	One-bit ripple-carry adder, drive strength 1
invzp_[1,2,4]	inverting tristate buffer, low enabled, drive strength 1, 2, or 4
ABnorC	(ip1*ip2+ip3)' drive strength 1
not_ab_or_c_or_d	(ip1*ip2+ip3+ip4)' drive strength 1
cd_16	clock driver, drive strength 16
lp_[1,2] high	active D latch, drive strength 1 or 2
lrsp_[1, 2, 4] high	active D latch with asynchronous low
dp_[1,2,4] rising	edge triggered D flip
drp_[1,2,4]	rising-edge triggered D flip-flop with asynchronous low-active reset (1, 2, or 4 drive strength)
jkcp_2	rising-edge triggered JK flip-flop with asynchronous active-low reset and extra inverted output, drive strength 2.

dtsp_1	rising-edge triggered D flip-flop with asynchronous active high set input and serial scan input.
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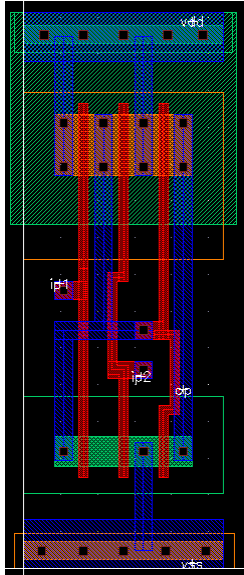


Figure 1: 2-input AND gate with driving strength 1

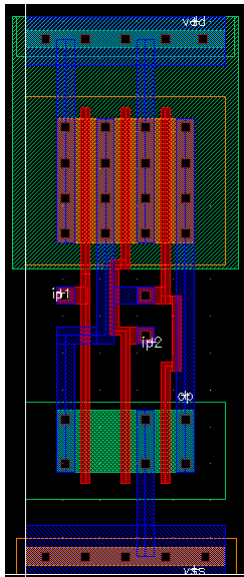


Figure 2: 2-input AND gate with driving strength 2

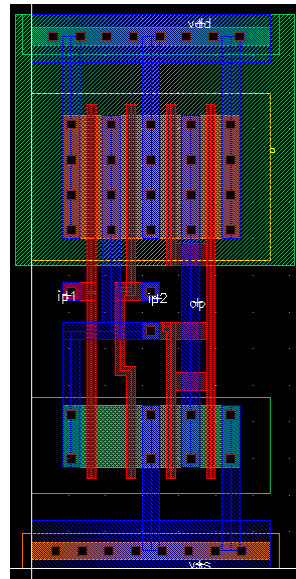


Figure 3: 2-input AND gate with driving strength 4

3. Cell Library Design

The major tasks for development of a cell library are: layout of cells, characterization, and LEF files generation. Our cells were laid out with Cadence Virtuoso and follow MOSIS DEEP rules (SCN5M_DEEP). TSMC 0.25 μm CMOS technology supports 5 metal layers, but the layout of cells is limited to only two metal layers, metal 1 and metal 2. This constraint allows P&R tools to use the remaining metal layers for routing. In addition to the design rules, the layout of cells follows rules shown in Table 2, which are necessary for P&R.

Table 2: Rules for Cell Layouts

Cell Design Settings	Values
Cell Height	108 λ
Cell Width	Multiple of 9 λ
Metal Pitch	9 λ for metal 1 through metal 4, 18 λ for metal 5
Metal Width	4 λ for all layers
Metal Offset	0 for all layers
Power/Ground Pins/Rails	11 λ for VDD and VSS

Note: λ is 0.12 μm .

Characterization of cells consists of capturing key parameters of cells such as propagation delay, rise and fall delays, and power dissipation. It was performed by extracting SPICE netlists from layouts and then simulating them using a SPICE simulator, HSPICE. The simulation results were ported into a .lib file and compiled by Synopsys Library Compiler for logic simulation and synthesis.

A LEF file for the cell library was generated for a P&R tool, specifically Cadence SOC Encounter. The extraction of abstract views and the generation of a LEF file were performed using Cadence Abstract. Mapping files, which enable Cadence Virtuoso to import the layouts from Cadence SOC Encounter, were generated manually based on the Cadence SOC Encounter mapping format.

5. Symbol Library

A symbol library allows users to view customized cell symbols rather than generic symbols, typically black boxes. Symbols were drawn using Cadence Virtuoso Schematic and Symbol editing tools. Then, symbols were exported into an EDIF file, which was compiled into an ASCII symbol library and eventually .sdb file using Synopsys Design Compiler, Figure 4 shows the process for generating a symbol library.

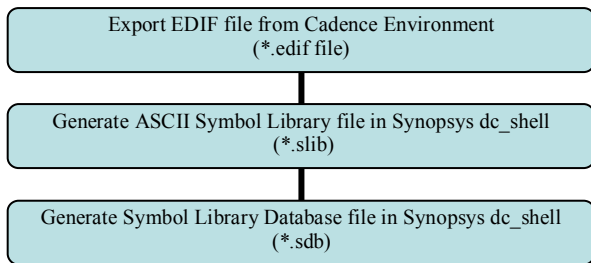


Figure 4: Generation of a Symbol Library

A symbol library also allows synthesized designs to be exported back from the synthesis tools into CAD tools for further design verification. This process of verification is part of the design flow approach that has been used by the VTVT Lab to test and use the standard cell libraries.

6. VTVT’s Design Flow Using the Standard Cell Library

The design entry is a VHDL description, which is simulated and then synthesized into a gate level netlist in verilog. The verilog netlist is imported into Cadence ICFB as a schematic view, and Cadence SOC Encounter performs P&R and generates the P&R layout view. Finally, the layout is verified against the synthesized schematic. The design flow is shown in Figure 5. For details, refer to [2].

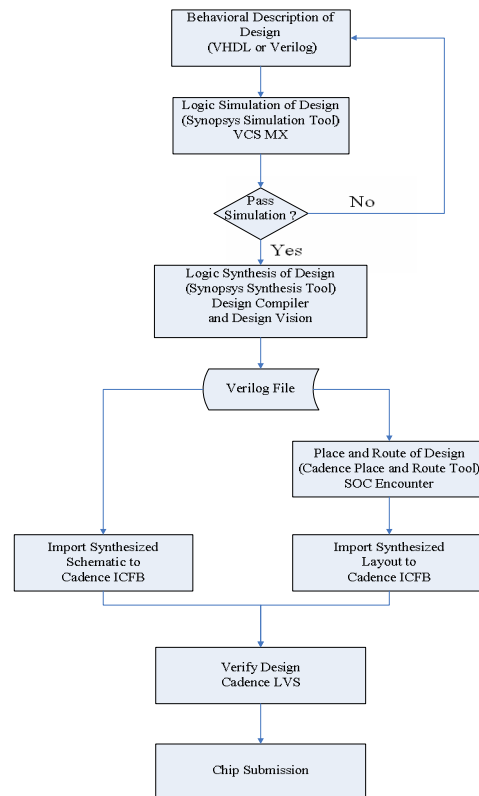


Figure 5: Design Flow Adopted by VTVT Lab

7. Summary

We presented basic features of TSMC 0.25 μm CMOS standard cell library developed by the VTVT lab and the design flow. We plan to develop cell libraries for more advanced technologies such as TSMC 0.18 μm and TSMC 0.10 μm and RAM compilers in the next two years. Finally, any university can obtain our cell library at no cost. For details, refer to [1].

Acknowledgement:

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References:

1. <http://www.vtvt.ece.vt.edu/vlsidesign/cell.php>
2. <http://www.vtvt.ece.vt.edu/vlsidesign/designFlow.php>