High Resolution Digital Duty Cycle Modulation Schemes for Voltage Regulators

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Abstract*-High switching frequency, high resolution digital pulse-width modulator (DPWM) is one of major challenges in the implementation of digital-controlled power converters, especially in the voltage regulator (VR) application. This paper proposes three different digital duty cycle modulation schemes to improve the resolution. Almost 10 times improvement on resolution can be achieved in the voltage regulator (VR) apparition. Design difficulty of the DPWM can be greatly reduced by proposed modulation schemes. Experimental results verify those modulation concepts.

***Keywords*- High resolution DPWM, limit cycle oscillation, voltage regulator**

I. INTRODUCTION

Due to the great progress made in the area of very-large-scale integration (VLSI), it is possible to broaden the application areas of digital control, especially in power electronics [1]. Digitalized control ICs can achieve several benefits, such as die size shrinking, passive components reduction, and cost saving. Furthermore, digital control provides many other functions: system management can be easily performed through the power management bus; advanced control algorithms make the possibilities for exploring the great potential in performance improvement; re-programmable and re-configurable capabilities can optimize the design for different applications flexibly. Digital power will become pervasive in the near future.

However, one of major challenges in digital control is quantization effects [2]. In the digital-controlled power converters, digital pulse-width modular (DPWM) and analog to digital (A/D) converter are two major quantizers. The duty cycle exported by DPWM can only have discrete values, and the resolution of the discrete duty cycle ultimately determines the resolution of the output voltage. If there is no desired output voltage value inside the zero-error bin of the A/D converter, limit cycle oscillations will happen. Ref. [3], [4]'s work show that high DPWM resolution can greatly reduce the limit cycle oscillations. Therefore, high-frequency, high-resolution DPWM design with reasonable power consumption and die size becomes the major challenges in the implementation of digital-controlled power converters [5].

In this paper, design challenge and a survey on the DPWM implementation are introduced in Section II. Then in Section III, three different high resolution digital duty cycle modulation schemes are proposed to address the design issue of the DPWM. Additional benefit in discontinuous mode (DCM) is investigated in Section IV. In Section V, experimental results verify the modulation concept. At last, summary is given in Section VI.

II. DESIGN CHALLENGE AND DPWM STRUCTURE REVIEW

As mentioned before, DPWM and A/D converter are introduced into the digital control loop, as shown in Fig. 1. On the one hand, the duty cycle resolution, ΔD, determines the resolution of output voltage, ΔV_o; on the other hand, A/D serves the purpose of digitalizing the analog output voltage into digital number with certain resolution, ΔV_{ADC}.

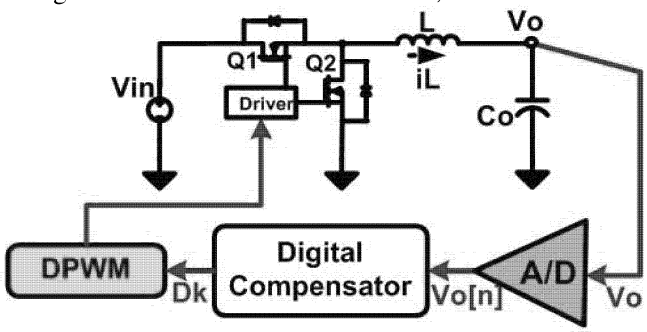

Fig. 1 Digital Controlled Buck Converter

The quantization effects of DPWM and A/D converter may result large magnitude limit cycle oscillation inside the loop. Limit cycle oscillation is hard to predicted and eliminated. However, If the resolution of the DPWM is sufficiently high, which makes $\Delta V_o < \Delta V_{ADC}$, limit cycle oscillations can be greatly reduced [3][4]. That's the reason why high resolution DPWM is very critical to digital controller design.

Many DPWM structures are proposed to achieve high resolution. The counter-based DPWM [5][6] is one of most

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common practices. In the counter-based DPWM, a counter is used to count the system clock cycle to determine the on-time and switching cycle. In this structure, the duty cycle resolution is determined by (1):

$$\Delta D = f_{sw} / f_{clock} \tag{1}$$

where, f_{sw} is the switching frequency of power stage and f_{clock} is the controller system clock frequency.

Taking the Buck converter as an example, the output voltage resolution in the continuous conduction mode (CCM) is determined by (2):

$$\Delta V_o = V_{in} \cdot \Delta D \tag{2}$$

where, V_{in} is the input voltage.

Fig. 2 shows the clock frequency requirement to achieve 3mV output voltage resolution under different switching frequency in the VR application (assuming V_{in} = 12V). As shown in the graph, even for 300-KHz VR, clock frequency has to be 1.2 GHz to meet the resolution requirement. Over GHz clock frequency is not feasible for practical implementation due to large power consumption. When the switching frequency goes higher, the situation becomes worse.

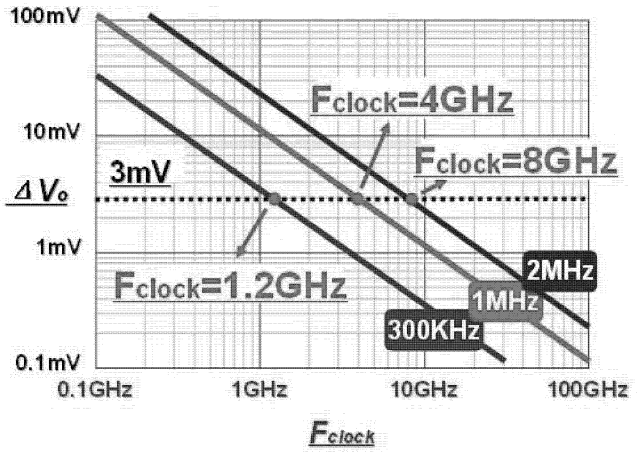

Fig. 2 System clock requirement

To deal with this problem, the hybrid DPWM [7]~[10] is proposed to lower down the system clock frequency by adding the delay-line structure, which consists of a series of delay cells. As shown in Fig. 3, system clock is used as the input to the delay-line:

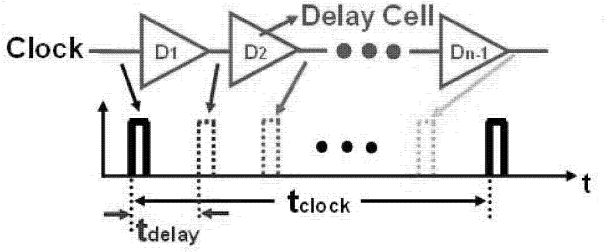

Fig. 3 Concept of hybrid DPWM

A delayed clock is generated after each delay cell. This time delay, t_{delay}, is much shorter than the system clock cycle, t_{clock}. Considering the multi-output of the delay-line, the clock frequency has been equivalently increased by n_d times with about n_d delay cells. The resolution of the hybrid DPWM, ΔD_{hybird}, is determined by (3):

$$\Delta D_{hybrid} = f_{sw} /(f_{clock} \cdot n_d) \tag{3}$$

Therefore, the hybrid DPWM can achieve much higher resolution than the counter-based DPWM with the same system clock frequency. The more the delay cells, the higher the resolution. However, extra silicon area is required by the delay-line, which results higher cost than the counter-based DPWM. Other than those two structures, dithering technique is introduced to increase the effective resolution of the DPWM [3][11], but the additional voltage ripple caused by the dithered duty cycle limits the benefits of this technique. Therefore, it is worth paying more efforts on the resolution improvement of DPWM for digital controlled power converters.

III. Proposed Digital Duty Cycle Modulation Schemes

A. DPWM Schemes

Similar to analog PWM modulation scheme, digital PWM has several schemes, such as trailing-edge modulation, leading-edge modulation and double-edge modulation, as shown in Fig. 4, where V_c is the output of the digital control compensator.

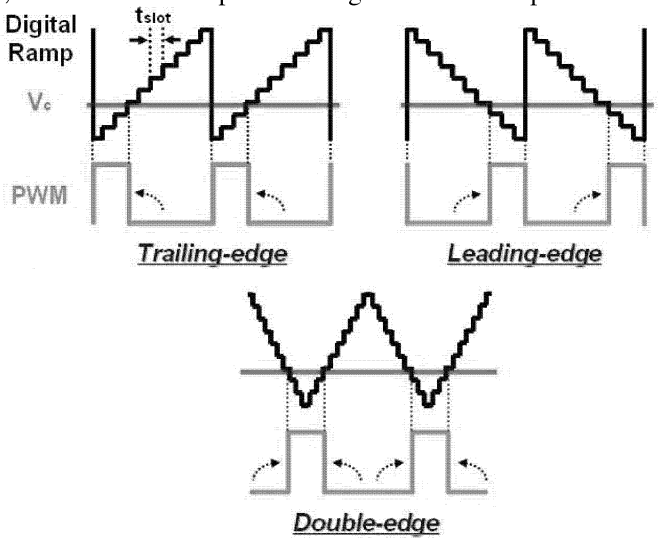

Fig. 4 DPWM modulation schemes

The difference is that digital ramp is used in the digital PWM while the analog ramp is used in analog PWM. The digital ramp is updated every time slot (t_{slot}), which is equal to t_{clock} (in the counter-based DPWM) or t_{delay} (in the hybrid DPWM).

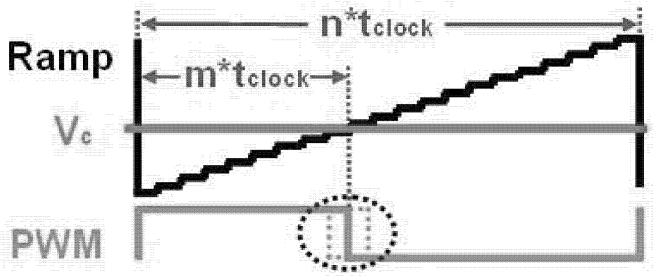

Fig. 5 Constant frequency modulation: trailing-edge modulation

If we take a close look at these three modulation schemes, all of them are constant frequency modulation. Nearly all existing DPWM structures are based on constant frequency modulation. In the following analysis, the counter-based DPWM with trailing-edge modulation is used as an example, as shown in Fig.5. Digital duty cycle can be express in (4):

$$D = (m \cdot t_{clock}) / (n \cdot t_{clock}) = m / n \quad (4)$$

where m and n are positive numbers. Because of constant frequency modulation, n is fixed for given switching frequency, while m is variable for different duty cycle values. The resolution can be easily calculated by (5):

$$\Delta D = m/n - (m-1)/n = 1/n \quad (5)$$

The higher the clock frequency is, the higher the n value, which means the higher duty cycle resolution.

B. Proposed Modulation Schemes

Different modulation schemes may give different duty cycle resolution. In the following paragraphs, three different modulation schemes are investigated.

(a) Proposed method #1 (Constant on-time modulation)

Method #1 is constant on-time modulation, as shown in Fig. 6. In the method #1, m is constant and n is variable, and duty cycle is expressed by (4).

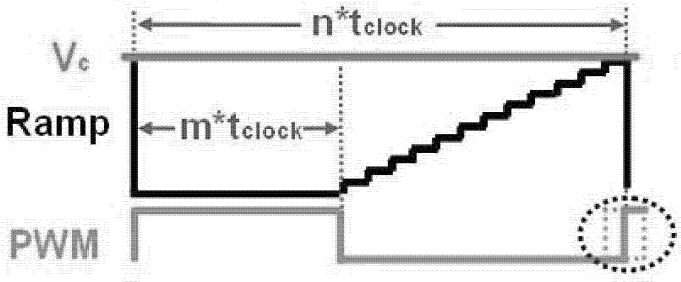

Fig. 6 Method #1: constant on-time modulation

The duty cycle resolution is obtained as (6):

$$\Delta D_{\#1} = \frac{m}{n} - \frac{m}{n+1} = \frac{m}{n(n+1)} \approx D \cdot \frac{1}{n} \quad (6)$$

Comparing with constant frequency modulation, the smaller the duty cycle is, the higher the resolution for constant on-time modulation. For Voltage Regulation (VR) application, steady state duty cycle is around 0.1, which means that about 10 times improvement can be achieved by changing the modulation scheme with the same system clock frequency.

(b) Proposed method #2 (Constant off-time modulation)

When the duty cycle is small, much higher resolution can be achieved in the method #1. However, when the duty cycle is close to 1, this advantage is not so promising. In order to overcome this problem, the method #2 is proposed. Method #2 is constant off-time modulation, as shown in Fig. 7.

In the method #2, p is constant and n is variable, and the duty cycle is expressed by (7):

$$D = (n - p)/n \quad (7)$$

The duty cycle resolution is obtained by (8):

$$\Delta D_{\#2} = \frac{(n+1)-p}{(n+1)} - \frac{n-p}{n} = \frac{p}{n(n+1)} \approx (1-D)\frac{1}{n} \quad (8)$$

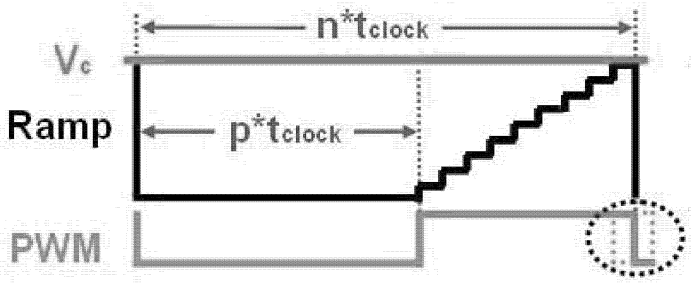

Fig. 7 Method #2: constant off-time modulation

Assuming f_{clock} = 150MHz, f_{sw} = 300KHz, duty cycle resolution comparison is shown in Fig. 8. Comparing with the constant on-time modulation, constant off-time modulation can achieve higher resolution when the duty cycle is close to 1. Method #1 and #2 are complementary with each other.

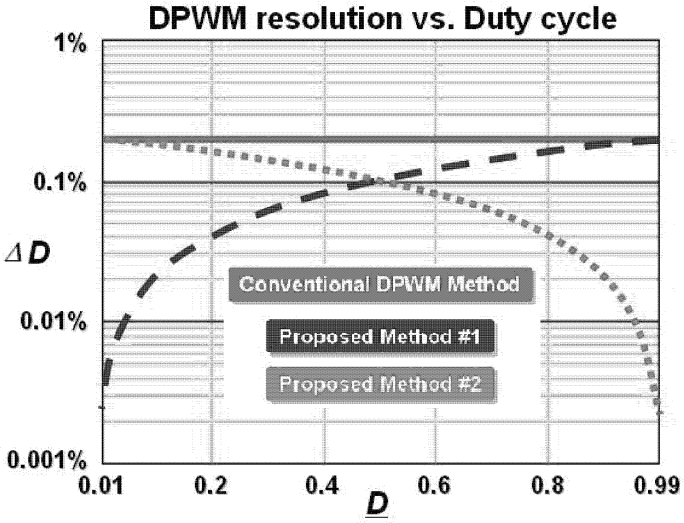

Fig. 8 Duty cycle resolution comparison

One concern about constant on-time and constant off-time modulation is switching frequency variation. For different duty cycle value, the switching frequency is different. This situation is severer in the laptop VR application, where the input voltage varies from 9V to 19V.

(c) Proposed method #3 (Nearly constant frequency modulation)

In order to overcome the drawback of variable switching frequency, Method #3 is proposed. Assuming duty cycle is close to 0, comparing with (5) and (6), it is found that changing m can achieve larger variation of duty cycle, while changing n can achieve smaller variation. Therefore, the method #3 is proposed based on the combination of constant frequency modulation and constant on-time modulation. In this method, duty cycle is expressed by (4), and m & n are both variable: changing m for coarse regulation; changing n for fine regulation. Because there is only a small variation on variable n, the switching frequency is almost constant for different duty cycle value. Fig 9 shows an example when D is about 0.2.

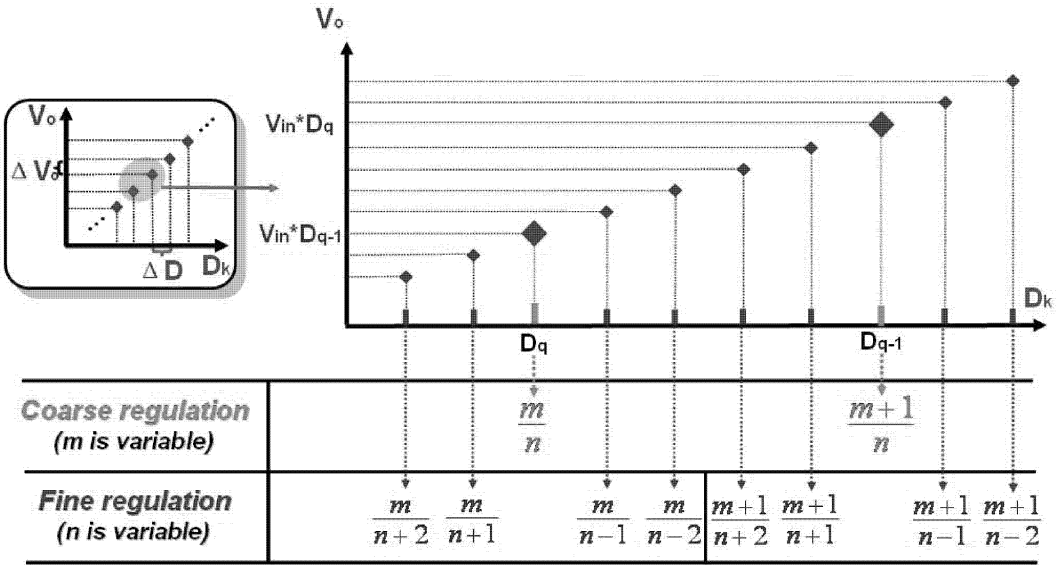

Fig. 9 Proposed method #3 when D = 0.2

Fig. 9 shows the relationship between the output voltage V_o and the duty cycle. D_q and D_{q+1} are two adjacent values achieved by coarse regulation, where m is variable. Therefore $D_q = m/n$, $D_{q+1} = (m+1)/n$. According to (6), the resolution can be increased about 5 times by changing n, since the duty cycle is about 0.2. Therefore, fine regulation is achieved as shown in Fig. 9. The variation of n is only 5, which guarantees the smallest switching frequency variation. For different duty cycle values, the variation of n is different.

Similarly, when duty cycle is close to 1, the method #3 is based on the combination of constant frequency modulation and constant off-time modulation.

C. *The Benefits of Proposed Modulation Methods*

Proposed modulation methods can greatly reduce the design difficulty of DPWM, especially for VR application. Assuming D is about 0.1, for the counter-based DPWM, the duty cycle resolution can be increased about 10 times based on the same system clock frequency; for the hybrid DPWM, due to 10 times higher resolution, delay cells can be reduced from the cost point view: with the same resolution, about 90% delay cell reduction can be achieved, which means significant cost reduction.

IV. Additional Benefits In DCM Operation

Continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are two basic operation modes for power supplies. This section investigates additional benefits of the proposed method #3 in DCM operation. For the Buck converter, V_o can be expressed by (9):

$$V_o = \begin{cases} V_{in} \cdot D & CCM \\ 2V_{in} \cdot (1+\sqrt{1+\frac{8L_s I_o}{V_o} \cdot \frac{f_{sw}}{D^2}})^{-1} & DCM \end{cases} \quad (9)$$

where I_o is the load current, L_s is the power stage inductor. And the duty cycle can be expressed by (10):

$$D = \begin{cases} \frac{V_o}{V_{in}}, & CCM \\ \sqrt{\frac{2L_s f_{sw} I_o}{V_{in} V_o}} \cdot \frac{V_o}{\sqrt{V_{in}-V_o}}, & DCM \end{cases} \quad (10)$$

As shown in (10), the duty cycle becomes smaller when load decreases at DCM operation. Assuming f_{sw} = 300KHz, V_{in} = 12V, V_o=1.2V, f_{clcok} = 150MHz, L_s = 600nH, Fig. 10 shows the duty cycle resolution comparison between constant frequency modulation and proposed modulation method #3.

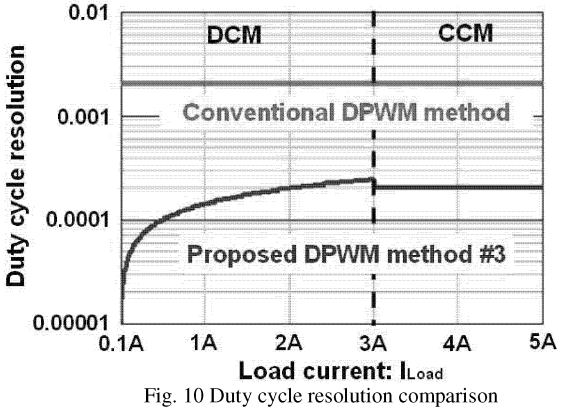

Fig. 10 Duty cycle resolution comparison

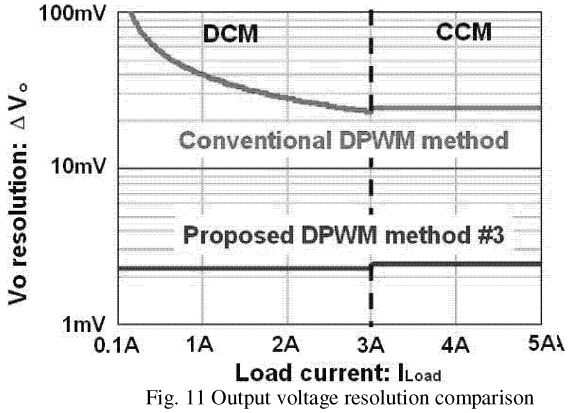

Fig. 11 Output voltage resolution comparison

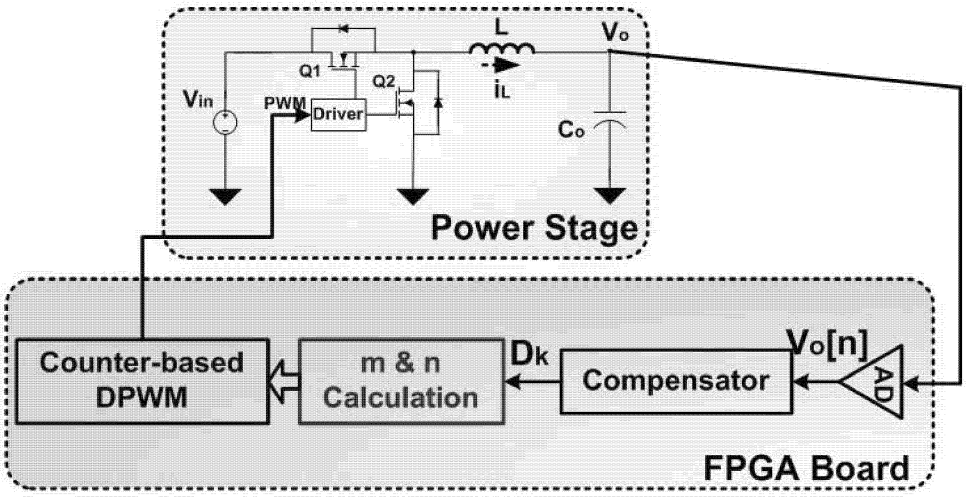

Fig. 12 Experiment setup

The relationship between output voltage resolution (ΔV_o) and duty cycle resolution (ΔD) is expressed by (11):

$$\Delta V_o = \Delta D \cdot \partial V_o / \partial D_{D=D_{ss}} \tag{11}$$

where D_{ss} is the steady state duty cycle. Based on (9), we can get (12).

$$\frac{\partial V_o}{\partial D} = \begin{cases} V_{in} & CCM \\ \sqrt{\dfrac{2V_o}{L_s I_o F_{sw}}} \cdot \dfrac{(1-V_o/V_{in})^{3/2}}{V_o/V_{in} \cdot (2-V_o/V_{in})} V_o & DCM \end{cases} \tag{12}$$

According to Equ (11 ~ 13), ΔV_o can be calculated and shown in Fig. 11. As shown in Fig. 11, proposed method #3 can achieve identical and much finer Δ Vo in both CCM and DCM, which is very promising for digital control system design.

V. Experimental Verification

Experiment verification has been done through Buck converter power stage and Xilinx Spartan II FPGA board with an additional ADC, as shown in Fig. 12. All parameters are as follows: V_{in} = 12V; V_{ref} = 1.2V; sampling frequency f_s = 300 KHz; switching frequency f_{sw} = 300 KHz; ADC resolution ΔV_{ADC} = 8mV, system clock frequency f_{clock} = 150 MHz.

(1) With the conventional counter-based DPWM: $\Delta V_o = V_{in} * \Delta D$ = 24mV, which is larger than ΔV_{ADC} (8mV); Based on Ref. [3, 4], there exists severe limit cycle oscillations on the output voltage V_o, as shown in Fig. 13.

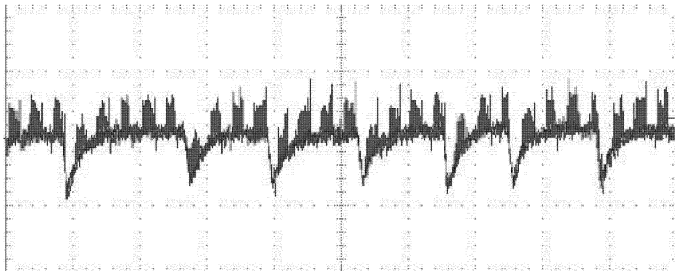

Fig. 13 V_o with the conventional DPWM (V_o: 10mv/div.; time: 4us/div.)

(2) With the proposed DPWM method #1: m = 50 (the on-time is about 0.33us), $\Delta V_o = V_{in} * \Delta D_{\#1}$ = 2.4mV, which is less than Δ V_{ADC} (8mV); Limit cycle oscillations can be greatly reduced, as shown in Fig. 14.

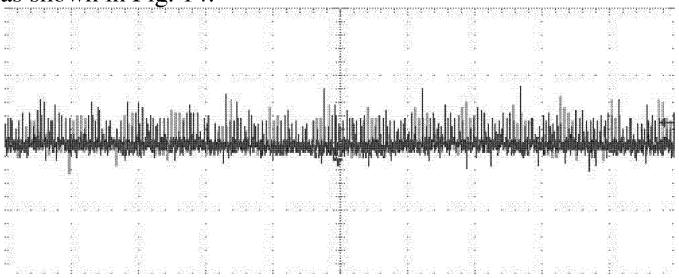

Fig. 14 V_o with the proposed method #1 (V_o: 10mv/div.; time: 4us/div.)

Because the proposed DPWM method #1 is constant on-time modulation, the switching frequency changes a lot at different conditions. Fig. 15 and Fig. 16 show the difference under different input voltage cases from inductor current iL waveforms.

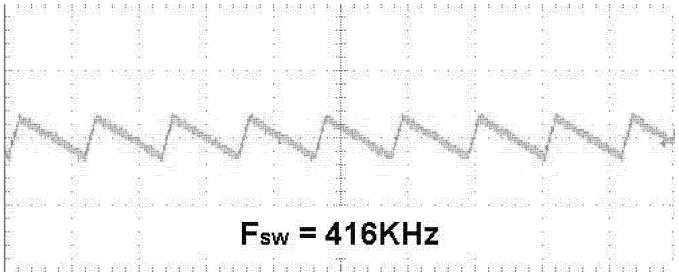

Fig. 15 i_L @ V_{in} = 8.7V (i_L: 5A/div.; time: 4us/div.)

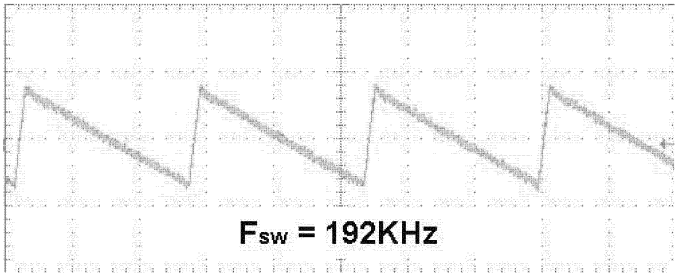

Fig. 16 i_L @ V_{in} = 19V (i_L: 5A/div.; time: 4us/div.)

With the proposed method #3, this issue can be solved, as shown in Fig. 17 and Fig. 18. Almost constant frequency is achieved by proposed method #3.

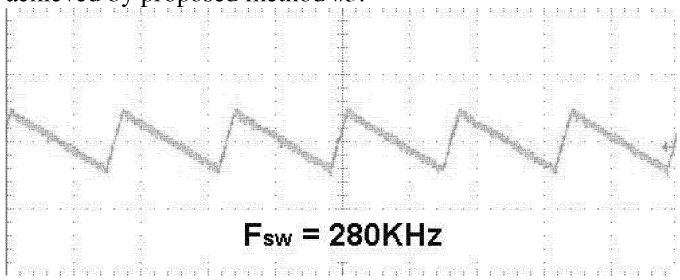

Fig. 17 i_L @ V_{in} = 8.7V (i_L: 5A/div.; time: 4us/div.)

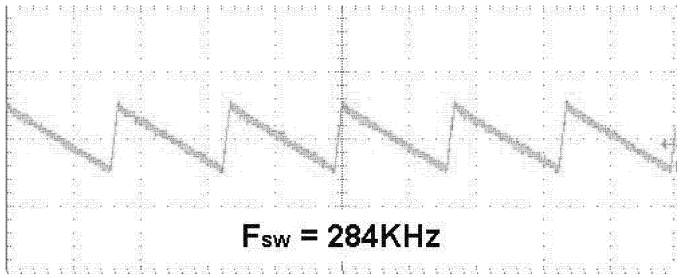

Fig. 18 i_L @ V_{in} = 19V (i_L: 5A/div.; time: 4us/div.)

VI. SUMMARY

High-frequency, high-resolution DPWM block is one of the major parts in digital controlled power converter systems. This paper proposed three kinds of high resolution DPWM methods. The proposed modulation schemes can achieve ten times finer resolution than the conventional DPWM in the VR application, which can greatly reduce the design difficulty of the DPWM. Experiment results verify the benefits.

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