Data Recovery Block Design for Impulse Modulated Power Line Communications in a Microprocessor

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Abstract

Power line communications (PLC) using impulse ultra wideband (UWB) in a microprocessor had been proposed for ubiquitous access of internal nodes for test/debug purposes. In this paper, we present a data recovery block, which is a key component for the proposed system. The data recovery block uses a novel sensing scheme, in which the sensing circuit's Power Supply Rejection Ratio (PSRR) is deliberately degraded. The proposed data recovery block was implemented in TSMC 0.18 μm CMOS process. Transient simulations indicate that our data recovery block can successfully recover data from a power line modulated with impulses with amplitude of about 90 mV and period of 300 ps. The proposed data recovery block consumes 2.8 mW when operating at a sampling rate of 1 GHz.

1. Introduction

As the complexity of a modern microprocessor increases rapidly and seemingly without bound, testing and debug strategies have to be constantly re-invented in order to keep pace with the complexity. Currently, there exists no systematic method to diagnose a system after it crashes and fails to reboot. Also, it is difficult to continuously monitor so called "large time-constant errors" i.e. errors that creep up over a period of time due to variations in temperature and simply aging. To support resilient operations in these contantly varying conditions, extensive monitoring is required throughout the entire die. Although self-test circuits are used to estimate these variations on a microprocessor die, most of the test circuits are either removed once the chip is deployed on the field or offer very limited access.

The Power Distribution Network (PDN) is ubiquitous across a microprocessor, i.e., a power line is accessible to any internal node. If a power line can be used to communicate with the external world, it can avoid preplanned routing of a data path from a node to an external data pin. This is a highly attractive feature for testing, as the routing of data paths is expensive in design time as well as in silicon area. The ability to monitor internal node values without routing data paths opens up a possibility for fault diagnosis, monitoring transient logic values during built-in self test, sending control data to sensors and for on-line testing.

Power line communications (PLC), patented in the early 1920's, has been mainly considered by utility companies for remote metering and control [3]-[4]. Recently, it has been revived for broadband internet access over existing power lines [5]. The use of power lines in an IC environment was introduced by the authors' group in [1] and extended to massive scan chains in [2]. As noted in [1]-[2], PLC in a microprocessor faces a totally different set of technical challenges from that of traditional PLC as described below. Most importantly, the noise characteristics as well as the communications channel of the power distribution network are completely different from a traditional PLC. Power lines consisting of a power distribution network are very noisy due to the so-called IR drop, Ldi/dt, and thermal noise [6]. Second, the signal power level at a power distribution network should be sufficiently small not to disturb the correct operation of the circuit, which makes the recovery of data from a noisy power line difficult. Such noise is not as much of problem for a traditional PLC. Finally, a microprocessor PDN is heavily decoupled to filter out the low frequency power supply noise as well as reduce the slew rate of current variations by locally supplying currents to switching nodes. Consequently, the PDN looks like a bulky low pass filter for high frequency signals. However, it is well known that the inductance in the decoupling capacitors becomes significant beyond the self resonant frequency of the capacitors. Also, at microwave frequencies (beyond 1 GHz) the PDN is essentially a distributed circuit and we observe

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some band of frequencies where the attenuation through the PDN is low [1] – [2]. This band of frequencies can be used for communication using impulse ultra wideband (UWB).

The rest of the paper is organized as follows. Section II describes the impulse UWB signaling over a microprocessor PDN, overall architecture of the PLC, and design considerations for the data recovery block. Section III describes the circuit-level implementation of the data recovery block. Section IV describes the performance evaluation of the proposed data recovery block and section V concludes the paper.

2. Preliminaries

This section describes signaling and modulation schemes for PLC, the overall architecture of the proposed power line communication method and issues involved in data recovery block design.

2.1. UWB signaling and Modulation scheme for PLC

Since the FCC's allocation of a UWB spectrum in the range of 3.1 GHz to 10.6 GHz in 2002, UWB has gained phenomenal interest in academia and industry [7]. Compared to traditional narrowband communication systems, UWB has several advantages such as high data rate, low average power, and simple RF circuitry. Shannon's theorem states that the channel capacity C is given as $B \times \log_2(1+SNR)$ [8], where B is the bandwidth. As the bandwidth B is much larger (on the order of several GHz) for UWB than for a narrowband signal, the SNR can be much smaller for UWB to achieve the same data rate. Therefore, with UWB communications one can often recover data, even if the signal power is close to the noise level. In other words, the power level of UWB signals could be at the noise level of power lines to have little impact to the power integrity.

UWB signaling can be carrier-based or impulse-based, and impulse UWB is more suitable for the proposed application due to its simple hardware [9]. Impulse UWB is based on train of narrow pulses (which are typically a few hundreds picoseconds wide). The most popular pulse shapes used for impulse UWB are Gaussian pulses and their derivatives [9]. Various modulation schemes such as on-off keying (OOK), pulse amplitude modulation (PAM), pulse position modulation (PPM) and binary phase shift keying (BPSK) are available for UWB. We adopt BPSK for sending data to the internal nodes due to its efficient performance. In this modulation scheme, the two possible bit values are represented by positive and negative going pulses. In the design of microprocessor PDN and decoupling solutions, the power supply variations are constrained within +/- 5% to maintain data integrity. Say, for a microprocessor with 1.8 V power supply; the amplitude of pulses on the PDN has to be less than 90 mV.

2.2. Overall Architecture

The overall architecture of the proposed PLC is shown in Figure 1. The impulse modulated data to be sent over the PDN can be applied on any of the power pins. The Data Recovery blocks (DR) are located at the various internal nodes. In addition to sending control data to a single sensor, different data can be sent to different sensors simultaneously using multiple access techniques borrowed from wireless communications, preferably Code Division Multiple Access (CDMA) so as to keep the data recovery digital friendly and simple.

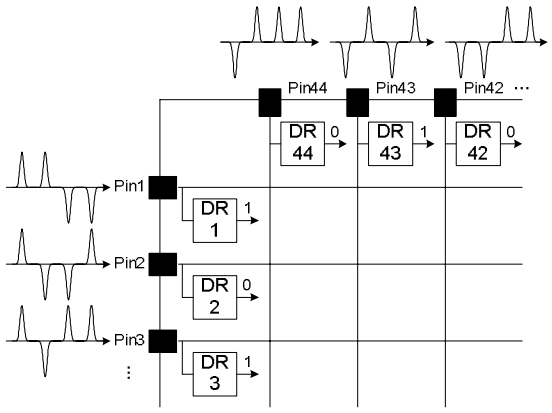

Figure 1. Overall architecture

2.3. Design Challenges of a Data Recovery Block

There are several challenges in the design of a data recovery block for communication over a microprocessor's PDN. Firstly, a data recovery block should be able to recover data from input signals whose voltage level exceeds its supply voltage (VDD). This is because the voltage level of a positive pulse imposed on the VDD is greater than the supply voltage of the data recovery block (which is also VDD). This situation is seldom encountered in circuit design. Secondly, the data recovery block should have high sensitivity with low offset, as the amplitude of pulses is small relative to the VDD level. Further, a microprocessor PDN is extremely noisy due to the enormous switching activity taking place in the die. Therefore the design should have high noise immunity. Finally, for the application

envisioned to be feasible, the design should be digital-process friendly with minimal area and power overhead.

3. Proposed Data Recovery Block

This section describes the circuit level implementation of our data recovery block and systematic transistor sizing for the sensing circuit.

3.1. Approach

From the perspective of a sensing circuit, narrow pulses superimposed on the supply voltage are high speed variations on the supply voltage level. Therefore, a sensing circuit has to translate the power supply voltage variation to a voltage variation offset by the output DC level of the sensing circuit. In fact, it is a common design practice to isolate the circuit output from power supply variations. Power Supply Rejection Ratio (PSRR) indicates the level of isolation of a circuit output from the power supply variations, and a larger PSRR is typically desired.

Our approach is to deliberately degrade the PSRR of a sensing circuit, so that the variations on the supply voltage level would appear at the sensing circuit output. We set the DC output voltage level of the sensing circuit at $0.5V_{DD}$, and a positive (negative) pulse on VDD will increase (decrease) the output voltage of the sensing circuit. The variation can then be amplified and regenerated to digital levels by a positive feedback latch. On the downside, degrading the PSRR would mean that accompanying power supply variations would also be transferred to the output of the sensing circuit. However, as long as the high speed variations offset by VDD are transferred to the circuit's output and the offset level is lowered the sensing scheme would suffice. Noise immunity can be improved by using strong coding (decoding) techniques.

The sensing scheme used for the proposed data recovery block is shown in Figure 2. It is a conventional common source amplifier with a diode-connected load. The input to the circuit is held at a constant voltage V_{bias}. A systematic sizing procedure for degrading the PSRR of the sensing circuit is described below.

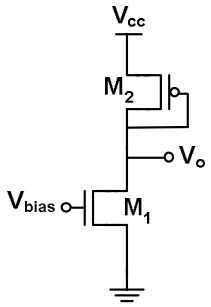

Figure 2. Sensing scheme

The PSRR of a common source amplifier shown in Figure 2 can be expressed as in (1).

$$PSRR = \frac{V_o}{V_{dd}} \approx \frac{1}{2 \cdot g_{m(M_2)} \cdot r_{o(M_1)}} \quad (1)$$

In-order to degrade the PSRR to its absolute worst, one has to maximize the product of $g_{m(M_2)}$ and $r_{o(M_1)}$. The transconductance of M_2, $g_{m(M_2)}$ is expressed as shown in (2).

$$g_{m(M_2)} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (2)$$

The output resistance $r_{o(M_1)}$ is expressed as in (3),

$$r_{o(M_1)} = \frac{1}{\lambda I_D} \quad (3)$$

From (2) and (3) we observe that the product $g_{m(M_2)} \cdot r_{o(M_1)}$ is inversely proportional to $\sqrt{I_D}$. Therefore, PSRR of the sensing circuit is degraded by reducing the current I_D through the sensing circuit.

However, the DC output voltage level of the sensing circuit is fixed at $0.5V_{DD}$ for regenerating the sensed pulse to digital levels. This, in turn, fixes the overdrive voltage of M_2. Therefore, the minimum current I_D is obtained by using minimum W/L ratio for M_2. The bias voltage V_{bias} and the W/L ratio of the M_1 are calculated to make sure that the transistor M_1 remains in saturation.

3.2. Overall Architecture

The entire data recovery block is shown in Figure 3. The sensing circuit is followed by a differential amplifier to amplify the sensed variations appearing at the sensing circuit output. The differential amplifier compares the sensed variation with a constant reference voltage V_{bias} and converts the single ended signal path to differential. By proper sizing of M_5 and M_6, the same voltage V_{bias} can be used as a reference voltage for the differential amplifier as well.

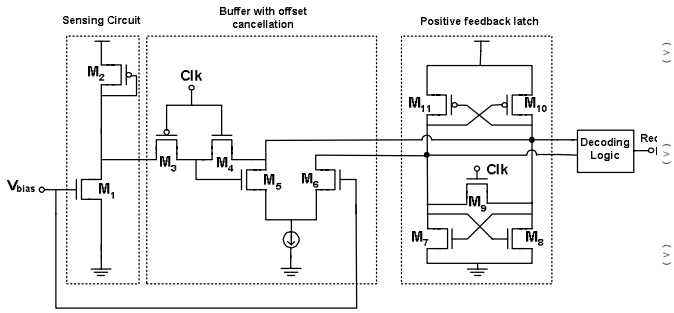

Figure 3. Data recovery block

Differential input to the latch helps to improve noise immunity as well as reduce the effect of offset variations. To reduce the effect of offset at the input of the latch, a conventional offset cancellation scheme is implemented using transistors M_3 and M_4. During the offset cancellation phase, with the clock high, M_4 is turned on, and the drain of M_5 is connected to its gate. Simultaneously, M_3 is turned off, and the gate of M_5 is isolated from the output of the sensing circuit. In this configuration, the input offset of the differential amplifier is stored in the parasitic gate-source capacitance of M_5 [10]. During the low-phase of the clock, the stored input offset is subtracted from the differential input and amplified. Finally, a positive feedback latch rapidly regenerates the differential amplifier outputs to digital levels. The built-in sampling switch M_9 in the latch samples the amplifier outputs at the falling edge of the clock. Inverter-based buffers are placed at the output of the data recovery block in-order to pull the output of the latch to the supply rails.

The clock for the data recovery block can be derived from the main microprocessor clock. A stable band-gap reference would be required to generate V_{bias} internally, and several data recovery blocks could share a single reference.

4. Performance Evaluation

4.1. Transient simulations

The proposed data recovery block was implemented and simulated with the target technology of TSMC 0.18 μm CMOS process under the supply voltage of 1.8 V. The variation in the power supply voltages were modeled using a piece-wise linear (PWL) source. In the definition of the PWL source, positive and negative going 90 mV pulses with duration of 300 ps were superimposed on the 1.8V level. Results of transient simulation are shown in Figure 4.

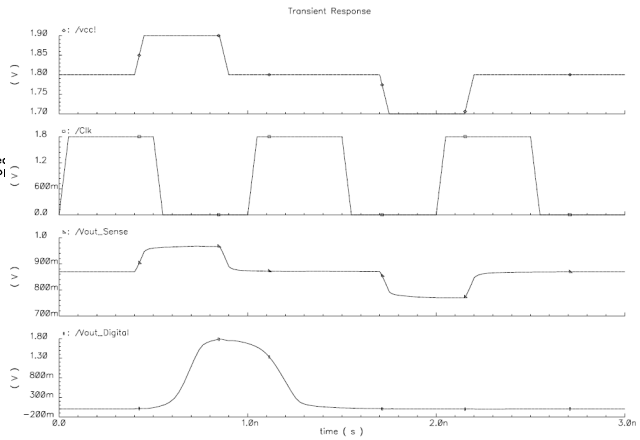

Figure 4. Operation of the data recovery block

The first waveform shows the PWL source on the global VDD, and the second waveform shows the sampling clock operating at 1 GHz. The third waveform shows the voltage at the output of the sensing circuit. It can be seen that the variations on the supply voltage are translated into the output signal variations. Also note that the DC voltage level of the sensing circuit output is set at 0.9 V. The last one shows the overall output of data recovery block. Note that positive pulses on the supply voltage are regenerated to logic '1's and negative pulses are regenerated to logic '0's.

The offset cancellation scheme implemented on the differential amplifier was evaluated using Monte Carlo analysis as well as mismatch and process variation models in the TSMC 0.18 μm process library [11]. With the process variations set at 3σ, the worst case offset observed at the input of the latch was less than 20 mV. The performance of the data recovery block is summarized in Table I.

Table 1. Performance summary

Pulse Amplitude	90 mV
Pulse Duration	300 ps
Clock Rate	1 GHz
Input Offset Variation	< 20 mV
Power consumption	2.8 mW

4.2. Effect of Noise in the PDN

The transient simulations shown in the previous section are simplistic in that a constant power supply voltage is assumed. In actuality, to evaluate the performance of a data recovery block, BER performance of the communication over the PDN should be investigated with a system level model by including power supply noise. Noise in the

microprocessor PDN can be broadly classified into three major components as described in [12].

- Cyclostationary background noise
- Strong deterministic components from the various clocks in the microprocessor.
- Low frequency (20 – 100 MHz) noise resulting from resonances in the PDN impedance characteristics.

To characterize random power supply noise reliably, one has to rely on measurements and empirical techniques. Some of the previously reported power supply noise measurements are also used to guide the noise modeling. The sampled variations measured on the power supply noise of an Itanium processor was reported in [13]. The average variation is less than $20mV_{p\text{-}p}$ (with a core supply voltage of 1.05V) but sampled noise voltage is observed over a range of ~ 70mV. Power Spectral Density (PSD) of power supply noise in a high-speed link transceiver was reported in [12]. In this ASIC, apart from the deterministic components, the power supply noise mostly appears white with a PSD of ~-30 dBV/Hz.

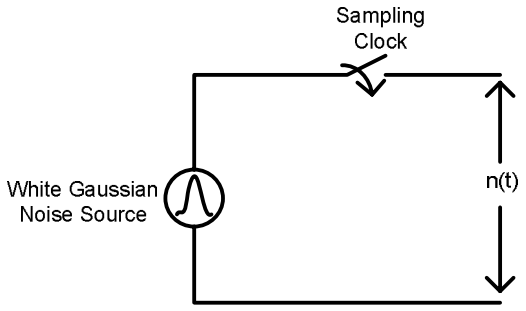

Figure 5. Gaussian cyclostationary noise model

Due to the enormous number of noise sources in a microprocessor, one can conclude that the overall noise will tend to a Gaussian process by the central limit theorem [8]. Also, since the majority of switching is periodic with respect to the main clock the noise can be considered to be cyclostationary Gaussian noise, which can be modeled as shown in Figure 5 [14]. Interference from internal clocks can be modeled deterministically with power levels comparable to reported measurement results [12]-[13]. Impulse based communications is fairly immune to low frequency noise from PDN impedance resonances so it is not included in the model.

However, since a complete system level model requires a PDN channel model as well as a behavioral model of the data recovery block, efforts to build a detailed system level model for performance evaluation is not yet complete.

5. Conclusion

A communication method using impulse UWB over the power distribution network in a microprocessor has been proposed in [1]-[2] for test/debug purposes. As a follow up step, a simple digital process friendly data recovery block is proposed to sample and latch the impulse modulated data. The proposed data recovery block was designed in TSMC 0.18μm CMOS process. From the simulations, we showed that information sent using pulses with peak amplitudes less than 5 percent of the power supply voltage can be received accurately using a data recovery block and sampling rate of the data recovery can be as high as 1 GHz. Further work is required to evaluate the performance of the data recovery block in the presence of power supply noise.

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