

Proposed DPWM Scheme with Improved Resolution for Switching Power Converters

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Abstract-Because of the need to eliminate the limit-cycle oscillations, a high-resolution DPWM scheme is mandatory, especially for the applications with high switching frequency and tight output regulation. Therefore, the dual-clock DPWM scheme is proposed in this paper. With two relative low frequency clocks, a much higher equivalent frequency is achieved for the DPWM; hence, the DPWM resolution is increased. With the proposed scheme, it is possible to implement the DPWM without delay lines even for high-frequency converters, which reduces the cost for the digital controller significantly. Experiment results based on a 300-kHz buck converter verify the improvement.*

Keywords- Limit cycle oscillation, dual-clock DPWM, digital control

I. INTRODUCTION

In recent years, the interest on digital control for switching power converters has grown considerably. When compared to its analog counterpart, the digital control approach has the potential to offer several advantages, such as the immunity to component variations, communication capability, the ability to perform sophisticated control algorithms and self-calibrations [1][2]. However, as the control target, the converter's power stage is mostly analog inherently [3]. Therefore, there exist several issues when implementing the digital control for the power converters [4]~[8].

One of major issues is quantization effects. In order to reduce limit cycle oscillations, high resolution digital pulse-width modular (DPWM) is mandatory for the system implementation. Several alternative solutions has been proposed, such as the delay-line based DPWM [5] [11], dithering DPWM [4]. Although the delay-line based DPWM can achieve much higher resolution than the counter-based DPWM, it requires large silicon area than the counter-based one. Moreover, the accuracy of the delay time of the delay cell is limited due to variations of the operating temperature,

manufacturing process, and the supply voltage. Ref. [13] proposes a solution with delay lock loop to minimize the nonlinearity of the delay cell. For the method of dithering DPWM, it increases the resolution by averaging several adjacent switching periods' duty cycle values; hence, a large-magnitude output ripple is resulted although the limit-cycle oscillation could be reduced [4].

In this paper, a DPWM scheme is proposed to improve resolution while keeping relative low cost. In Section II, design challenge of DPWM is introduced. Then, proposed dual-clock DPWM scheme is investigated in Section III. Detail implementation is discussed in Section IV. In Section V, some experimental results verify proposed concept.

II. DESIGN CHALLENGE OF DPWM

Fig. 1 illustrates the structure of a buck converter with voltage-mode digital control, where the digital pulse-width modulator (DPWM) and the analog-to-digital converter (ADC) serve as the interfaces between the analog power stage and the digital controller.

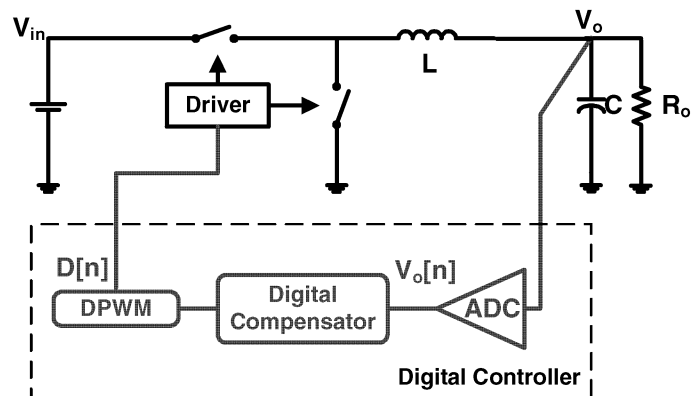


Fig. 1 A Buck converter with voltage-mode digital control

Because of the inherent digital characteristics, there exist quantization effects in the DPWM and the ADC [4]: only discrete values are obtained at their outputs. As the result of the quantization effect of the DPWM, only limited resolution of the duty cycle, D , can be obtained. Consequently, the output voltage also has limited resolution, V_{o_DPWM} :

$$\Delta V_{o_DPWM} = V_{in} \cdot \Delta D \quad (1)$$

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It has been observed and analyzed that a large-magnitude limit-cycle oscillation might happen at the output voltage if V_{o_DPWM} is not as fine as that of the ADC, V_{ADC} , i.e.,

$$\Delta V_{o_DPWM} > \Delta V_{ADC} \quad (2)$$

as shown in Fig. 2 [4]~[6]. This limit-cycle oscillation is a severe concern for switching power converters, especially for the application requiring tight output regulation.

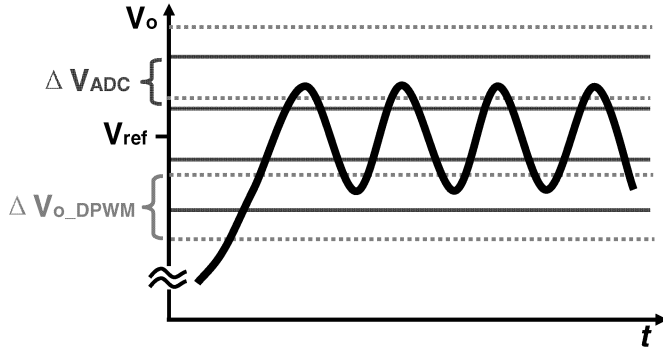


Fig. 2 Limit cycle oscillation with insufficient DPWM resolution

Another challenge to the DPWM design comes from the converter's switching frequency because the duty cycle resolution is determined by:

$$\Delta D = t_{clock} \cdot f_s \quad (3)$$

where t_{clock} is the digital controller's system clock cycle, and f_s is the converter's switching frequency. To obtain the same V_{o_DPWM} to avoid the limit-cycle oscillation, a higher switching frequency converter demands a faster digital controller system clock, which also poses stringent challenges on the DPWM design.

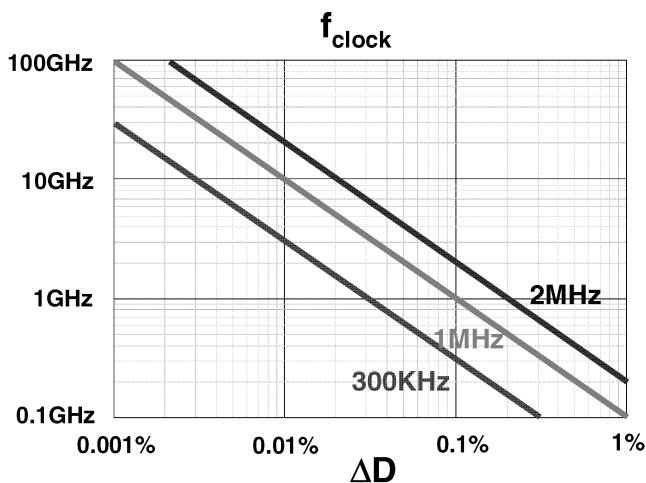


Fig. 3 Digital controller's required system clock frequency to avoid limit-cycle oscillation

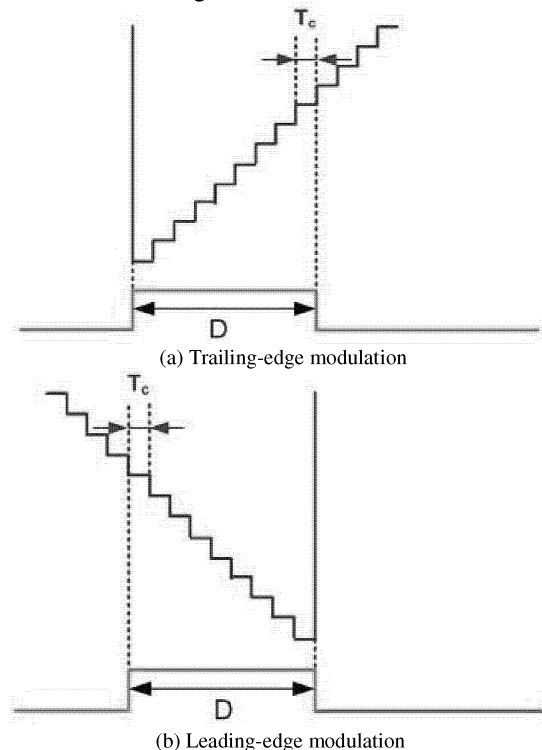
Fig. 3 illustrates the relationship between the duty cycle and the required controller clock frequency under different switching frequencies. If a 3-mV output resolution is desired with 12-V input for the buck converter, a 0.025% duty cycle resolution is required. As a result, if the switching frequency is 300 kHz, a 1.2-GHz system clock is needed for the digital

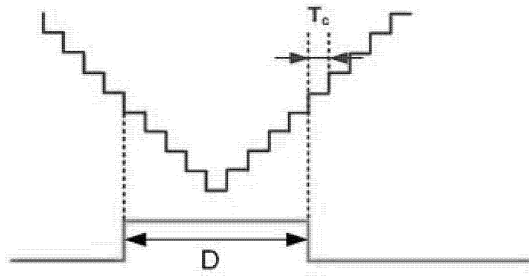
controller. If the switching frequency is 2 MHz, an 8-GHz system clock is needed. Therefore, in the applications that require both tight output regulation and high switching frequency, such as voltage regulators or other point-of-load converters, high DPWM resolution is one of the major concerns for the digital power controller designers [4][9]~[12].

To deal with the issue of extreme high clock frequency of the digital controller, there are several alternative solutions proposed, such as the delay-line based DPWM [5][11], dithering DPWM [4], etc. With the delay-line based structure, the DPWM minimal time slots are generated by the propagation delay of a pulse through delay cells, and then selected by MUX to produce PWM output. Compared with the conventional counter-based structure, where the time slot is equal to the system clock, the delay-line based structure requires much lower system clock frequency but a larger silicon area [5]. Meanwhile, the accuracy of the delay time is limited due to variations of the operating temperature, manufacturing process, and the supply voltage. For the method of dithering DPWM, it increases the resolution by averaging several adjacent switching periods' duty cycle values; hence, a large-magnitude output ripple is resulted although the limit-cycle oscillation could be reduced [4]. Therefore, more efforts are desired for the high-resolution DPWM methods in the digital power controller designs.

III. PROPOSED DUAL-CLOCK DIGITAL PWM SCHEMES

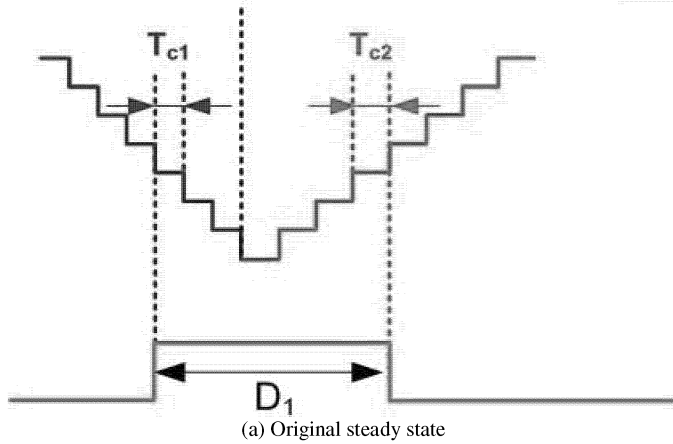
To investigate the possibility of DPWM resolution improvement from the modulation schemes aspect, Fig. 4 compares three popular modulators: leading-edge, trailing-edge and the double-edge PWM.



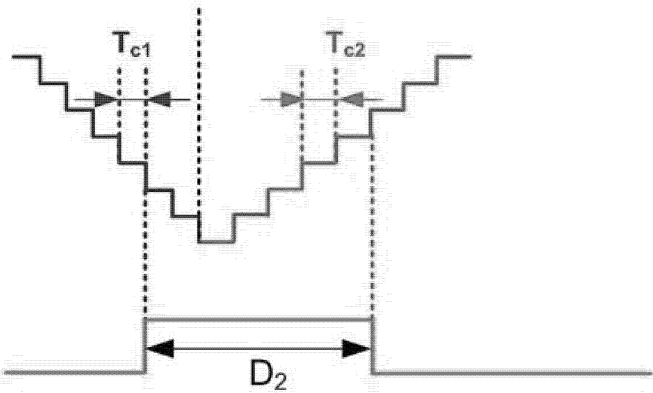


(c) Double-edge modulation
Fig. 4 DPWM modulation schemes

Similar to the analog PWM, the DPWM functions utilize a control signal, V_c , to compare with the PWM ramp. Because of the advantages of sampling with double-edge modulation, it has been widely used in the industry applications. The implementation difference from trailing-edge and leading-edge schemes is that it has both the rising and the falling digital ramp. However, the rising and falling slope are equal in the previous designs. Although it is a simple solution, those designs have not fully utilized the flexibility of double-edge modulation. If the relationship between the two slopes is to be designed, there is one more parameter to control the DPWM resolution.



(a) Original steady state



(b) Next steady state

Fig. 5 Preliminary dual-clock DPWM scheme

Based on this concept, in this paper, the dual-clock DPWM scheme is proposed with double-edge modulation. Fundamentally, this method utilizes two clocks, T_{c1} and T_{c2} , for the falling and rising PWM ramps respectively, as shown in Fig. 5, where T_{c2} is slightly longer than T_{c1} . Therefore, with the combination of the two time slots at different edges, it is possible to obtain a much higher equivalent frequency for the DPWM.

For example, as shown in Fig. 5, from the original steady state to the next steady state, instead of increasing the time slots in both the falling and the rising ramp simultaneously as the conventional method, the dual-clock DPWM reduces one T_{c1} slot at the falling slope, but increases one T_{c2} slot at the rising slope. As the result, the duty cycle variation is

$$D_2 - D_1 = (T_{c2} - T_{c1}) \cdot f_s \quad (4)$$

Therefore, the minimal time slot determining the DPWM resolution is:

$$T_{slot} = T_{c2} - T_{c1} \quad (5)$$

which means that the equivalent frequency is increased to

$$f_{clock} = (f_{c1} \cdot f_{c2}) / (f_{c2} - f_{c1}) \quad (6)$$

where f_{c1} and f_{c2} are the frequencies for the two system clocks.

However, based on the concept in Fig. 5, it is impossible to obtain the desired DPWM resolution over the entire duty cycle range. Once the falling ramp time slot is decreased to zero, the DPWM resolution is T_{c2} if next larger duty cycle is demanded. Therefore, a modified approach is proposed as in Fig. 6, where one switching cycle, T_s , have integer numbers of T_{c1} and T_{c2} slots, and the first clocks of them are synchronized.

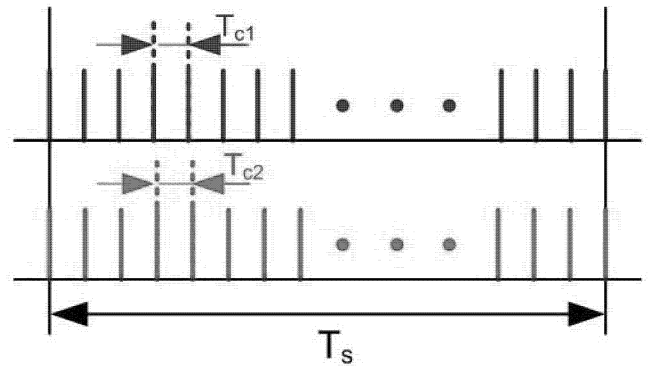


Fig. 6 Dual-clock DPWM scheme

For example, if T_s have N T_{c1} slots and M T_{c2} slots, and the original duty cycle contains the first K T_{c2} slots in T_s , the duty cycle is

$$D_0 = K / M \quad (7)$$

Then, the next larger duty cycle is obtained by using the second T_{c1} clock as the leading edge of the duty cycle, and the $(K+2)$ -th T_{c2} clock as the trailing edge. Therefore, the next duty cycle is

$$D_1 = K / M + (T_{c2} - T_{c1}) / T_s = K / M + (1 / M - 1 / N) \quad (8)$$

Following the same concept, with P $(T_{c2} - T_{c1})$ time slots added to the duty cycle,

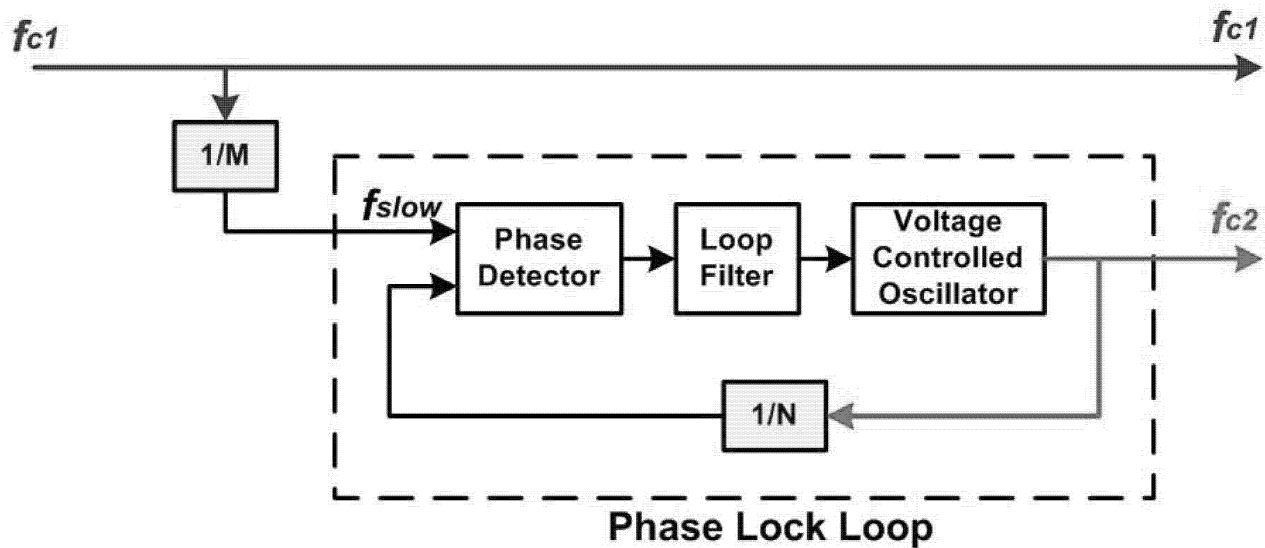


Fig. 7 Implementation of Dual-clock DPWM scheme

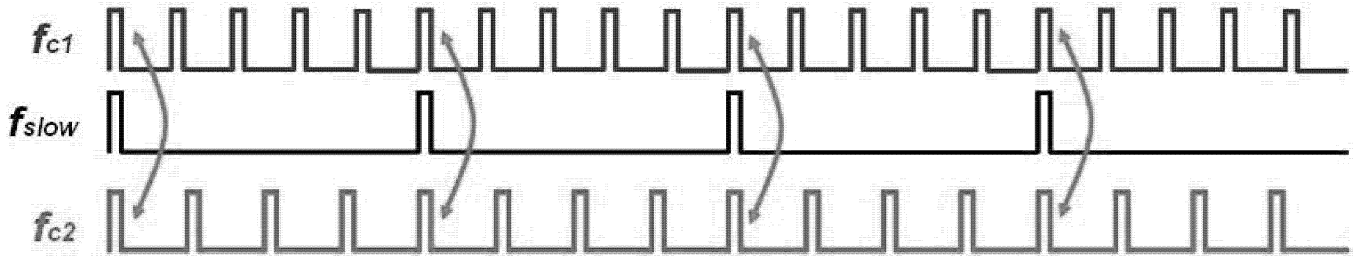


Fig. 8 Two clocks generation and synchronization with $M = 5$ and $N = 4$

$$\begin{aligned}
 D_p &= K/M + P(T_{c2} - T_{c1})/T_s \\
 &= K/M + P(1/M - 1/N) \\
 &= (K + P(N - M)/N)/M
 \end{aligned} \tag{9}$$

therefore, if $P=N/(N-M)$, $D_p=(K+1)/M$, which is equivalent to increase one T_{c2} slot. Hence, the DPWM resolution is increased over all the duty cycle range except for extreme large and extreme small cases. A special case is that $N=M+1$, $P=N$, which means that after wrapping the duty cycle around one switching period, the duty cycle resolution of $(T_{c2}-T_{c1})/T_s$ is perfectly realized over the entire duty cycle range.

From the previous analysis, the leading and the trailing edges of the duty cycle are both variable. It is possible for the duty cycle to shift around in one switching cycle. In order to limit the shifting, two clocks can be designed to meet (10):

$$T_s = R \cdot (M \cdot T_{c1}) = R \cdot (N \cdot T_{c2}) \tag{10}$$

where R is positive number. The larger the R is, the smaller the shifting. In Section IV, a simple example is given to further explain this concept.

IV. IMPLEMENTATION OF PROPOSED SCHEME

To implement the proposed dual-clock DPWM scheme, there are three additional functions needed. First, the digital controller calculates the desired combination of two different time slots. This function can be easily realized just by modifying the DPWM software. Second, an additional clock is

needed, which might increase the cost. Third, the synchronization of the two clocks is needed. For the second and third, it can be implemented by phase lock loop (PLL) with just one clock input, f_{c1} , as shown in Fig.7. f_{c1} is one of clocks which is produced by oscillator; then, f_{c1} is divided by M times to get a much slower clock f_{slow} ; then, f_{slow} is multiplied by N times based on PLL. Fig. 8 shows an example with $M = 5$ and $N = 4$. Two clocks are synchronized with f_{slow} , and $T_{slot} = T_{c2} - T_{c1} = (1/5)T_{c2}$. Duty cycle generation is shown in Fig. 9. Assuming the starting duty cycle $D_0 = (3T_{c2})/T_s$, and rising edge and falling edge are both determined by the clock 2. Based the concept proposed before, the next adjacent duty cycle $D_1 = (3T_{c2}+T_{slot})/T_s$. To generate this duty cycle, the second rising edge of the clock 1 determines the rising of the duty cycle, and the $(3+2)$ th rising edge of the clock 2 determines the falling edge of duty cycle. From the clock number point view, it is like shift one clock for two clocks. Because the equivalent clock frequency is 5 times of f_{c2} , so that five clocks could be shifted, as shown in Fig. 5. After shifting five clocks, the duty cycle $D_5 = (3T_{c2}+5T_{slot})/T_s = (4T_{c2})/T_s$, so that it can also be produced by four T_{c2} , and starts at the first clock. Comparing D_0 and D_4 , the maxim shift timing is about $4 T_{c1}$. In the real application, shifting timing is needed to be designed based on different requirements, especially for those with fast transient requirements. Moreover, for multi-phase application, phase shift could be achieved based on the slow clock.

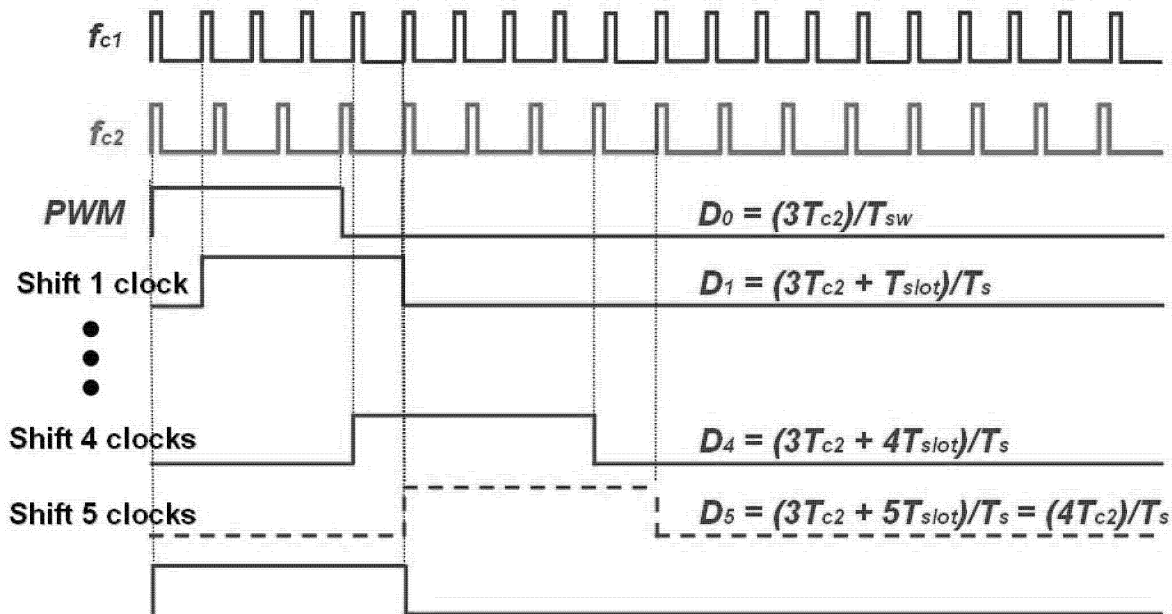


Fig. 9 Duty cycle generation based on two clocks

Considering the PLL is also needed for the conventional DPWM structure with delay lines [13], the digital controller's die size can be significantly reduced by removing the delay line cells. As an example, Table 1 compares the hardware requirement for the conventional and the proposed schemes to realize 10-GHz DPWM resolution. A 90% saving of the silicon area is achieved with the proposed scheme. Therefore, from the system aspect, the dual clock method has more advantages over the conventional one. Therefore, from the system aspect, the dual clock method has more advantages than the conventional one.

TABLE 1 Comparison of the DPWM schemes.

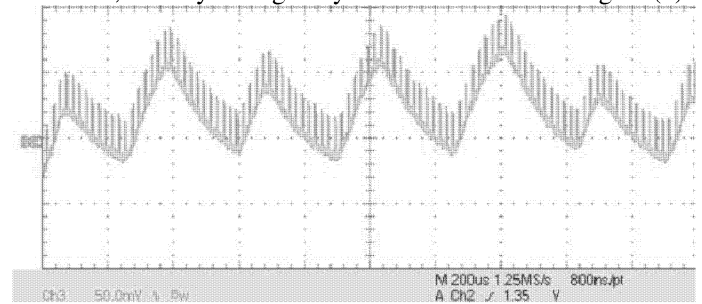
DPWM Schemes	Clock Frequency	Delay Cell	PLL	Die Size [4][12]
Counter + delay line	100 MHz	100	Yes	1.1 mm ²
Dual clock	100 MHz & 101 MHz	0	Yes	0.1 mm ²

According to (5) and (6), it is desired to set the two clocks' frequencies as close as possible for a higher DPWM resolution. However, with closer frequencies, a higher accuracy of the clock generators is required, and it is more difficult to synchronize them with PLL. Therefore, a trade off exist in the design. After detailed study, it is found to be a good compromise between the cost and performance when the difference of the two clocks is controlled around 1~10 MHz.

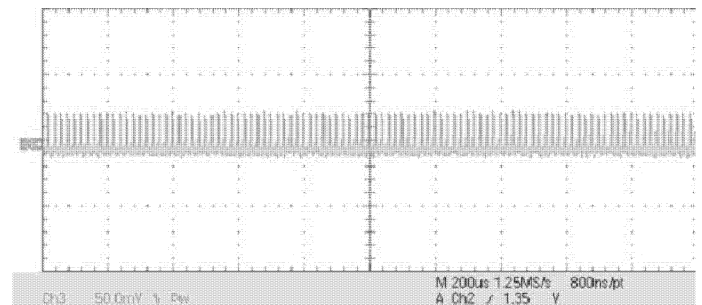
V. EXPERIMENT VERIFICATION

To verify the proposed DPWM scheme through experiment, a digital control buck converter with 12-V input, 1.2-V output, and 300-kHz switching frequency. The digital controller is realized using Spartan II FPGA from Xilinx. The ADC resolution is 32 mV.

Fig. 10 compares the output voltage waveform of the conventional DPWM with a 30-MHz clock and the dual-clock DPWM with 25-MHz and 30-MHz clocks. For the conventional DPWM, $V_{o_DPWM} = 12/100 = 120mV$, which is much larger than the ADC resolution, so that limit cycle oscillation is severe at the output as shown in Fig. 10(a). On the other hand, because the equivalent clock frequency is increased to 150 Mhz, $V_{o_DPWM} = 12/500 = 24mV$. In this condition, limit cycle is greatly reduced as shown in Fig. 10(b).



(a) Limit-cycle oscillation with a 30-MHz clock.



(b) Elimination of limit-cycle oscillation with 25-MHz and 30-MHz dual-clock DPWM scheme.

Fig. 10 Output voltage waveform: improvement of the duty cycle resolution with the proposed DPWM scheme

VI. SUMMARY

In summary, because of the need to eliminate the limit-cycle oscillations, a high-resolution DPWM scheme is mandatory, especially for the applications with high switching frequency and tight output regulation. Therefore, the dual-clock DPWM scheme is proposed in this paper. With two relative low frequency clocks, a much higher equivalent frequency is achieved for the DPWM; hence, the DPWM resolution is increased. With the proposed scheme, it is possible to implement the DPWM without delay lines even for high-frequency converters, which reduces the cost for the digital controller significantly. Experiment results based on a 300-kHz buck converter verify the improvement.

REFERENCES

- [1] A. Peterchev, J. Xiao, S. Sanders, "Architecture and IC Implementation of a Digital VRM Controller," *IEEE Transactions on Power Electronics*, pp. 356-364, Jan. 2003.
- [2] D. Maksimovic, R. Zane, R. Erickson, "Impact of Digital Control in Power Electronics," *IEEE International Symposium on Power Semiconductor Devices & ICs*, pp. 13-22, 2004.
- [3] S. Pietkiewicz, "Digital Power Is Mostly Analog," *Power Electronics Technology Magazine*, Jan. 2006.
- [4] A. Peterchev, S. Sanders, "Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters," *IEEE Transactions on Power Electronics*, pp. 301-308, Jan. 2003.
- [5] A. Syed, E. Ahmen, E. Alarcon, D. Maksimovic, "Digital Pulse-Width Modulator Architectures," *IEEE PESC*, Vol. 6, pp. 4689-4695, 2004.
- [6] H. Peng, D. Maksimovic, A. Prodic, E. Alarcon, "Modeling of Quantization Effects in Digitally Controlled DC-DC Converters," *IEEE PESC*, pp. 4312-4318, 2004.
- [7] O. Trescases, Z. Lukic, W. Ng, A. Prodic, "A Low Power Mixed-Signal Current-Mode DC-DC Converter Using a One-bit Delta Sigma DAC," *IEEE APEC*, pp. 700-704, 2006.
- [8] M. Ferdowsi, "An Estimative Current Mode Controller for DC-DC Converters Operating in Continuous Conduction Mode," *IEEE APEC*, pp. 1133-1136, 2006.
- [9] A. Wu, J. Xiao, D. Maksimovic, S. Sanders, "Digital PWM Control: Application in Voltage Regulation Modules," *IEEE PESC*, pp. 77-83, 1999.
- [10] A. Syed, E. Ahmed, D. Maksimovic, "Digital PWM Controller with Feed-Forward Compensation," *IEEE APEC*, pp. 60-66, 2004.
- [11] B. Patella, A. Prodic, A. Zirger and D. Maksimovic, "High-Frequency Digital PWM Controller IC for DC-DC Converters," *IEEE Transactions on Power Electronics*, pp. 438-446, Jan. 2003.
- [12] J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE Journal on Solid State Circuits*, pp. 1723-1732, Nov. 1996.
- [13] V. Yousefzadeh, T. Takayama, D. Maksimović, "Hybrid DPWM with Digital Delay-Locked Loop," *IEEE COMPEL*, June 2006.