Off-time Prediction in Digital Constant On-time Modulation for DC-DC Converters

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***Abstract*—This paper proposes a digital constant on-time control method for high switching frequency DC-DC buck converter, which eliminates the need for high resolution digital pulse-width modulator (DPWM) compared to constant frequency control. Both simulation and experimental results demonstrate performance improvement through the proposed off-time prediction method in terms of the oscillation amplitude of the output voltage.**

I. INTRODUCTION

Digital control for high-frequency (e.g. hundreds of kilohertz to megahertz) switched-mode power supplies has gained increased attentions recent years due to a number of potential advantages [1-3]. A digital controller has lower sensitivity to parameter variations compared to its analog counterpart; therefore digital solution is a better option when the controller demands high precision such as in controlling multiphase converters. Digital control can be configured flexibly to meet the requirements of different applications, and the digital interface makes it easy to communicate with a power management system. Furthermore, through advanced digital control algorithms, it is possible to improve system performance in terms of efficiency and speed. Fig. 1 shows the architecture of a digital voltage-mode controller for buck converter.

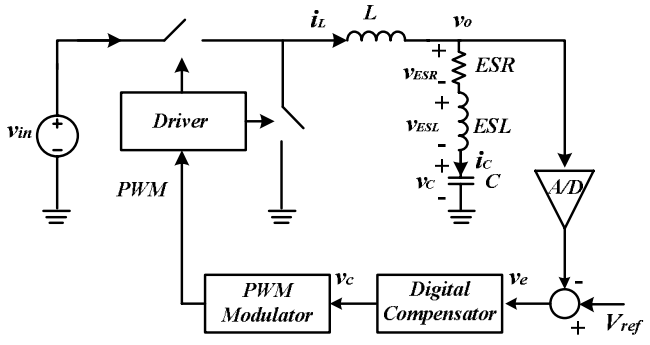

Figure 1. Digital voltage-mode control for a buck converter.

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However, there are still some critical challenges when applying digital control to high-frequency switched-mode power supplies. Among them, the limit cycle oscillation caused by quantization process (such as due to an A/D converter) in the feedback loop is the major problem. Unlike analog control, the resolution in a digital control loop has a finite value resulting from the quantizing elements in the system -- the A/D converter and the DPWM (which serves as a D/A converter). Duty cycle modulated by DPWM can only be discrete values and the resolution of DPWM ultimately determines the resolution of output voltage. Therefore if there is no DPWM level based on which the system can drive the output voltage to A/D converter's zero-error bin, the system will bounce up and down around the desired value [4,5]. The amplitude and frequency of this limit cycle oscillation is hard to predict and confine. Reduction of the limit cycle oscillation requires high resolution DPWM. Several techniques have been proposed to increase modulation resolution, such as dithering technique [4,6], delay-line-based DPWM [7] and hybrid DPWM[3,8] (which is a combination of counter-based structure and delay-line structure). Besides the traditional constant frequency control, Li et al. proposed voltage-mode digital constant on-time modulation method and constant off-time method, which achieve significant improvement on the resolution of DPWM [9]. Recently, a digital current-mode constant on-time control through V^2 control architecture has been proposed [10], which limits the influence of the limit cycle oscillation. Additional digital ramp is added to further lower down oscillation amplitude, but the dynamic performance suffers because the modulation gain is decreased due to the additional ramp.

This paper proposed a prediction method to address the above shortcoming. The feasibility and advantages of digital current-mode constant on-time control are analyzed in the Section II. In Section III, the off-time prediction method is proposed to further reduce the limit cycle oscillation amplitude. This proposed algorithm is verified through simulation and experimental results in the Section IV. A conclusion is given in Section V.

II. DIGITAL CURRENT-MODE CONSTANT ON-TIME CONTROL

The output voltage of a buck converter is filtered through an L-C network. Because of the parasitic resistance and inductance on the output bulk capacitor, i.e. the equivalent series resistor (ESR) and equivalent series inductor (ESL), the output voltage always has small ripple. Fig. 2 shows the voltage ripple on output capacitor during steady state. Δi_L in the figure is the peak-to-peak value of inductor current.

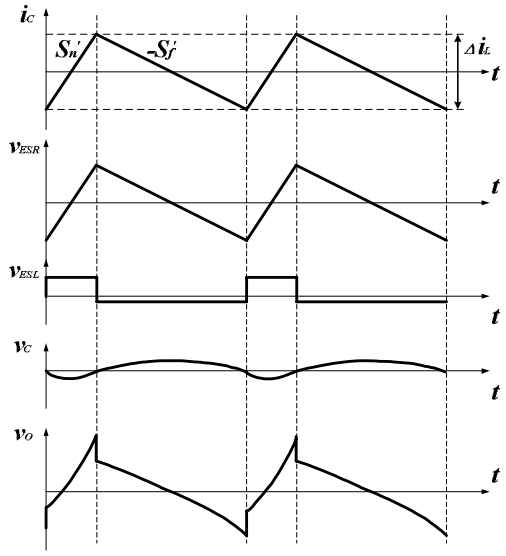

Figure 2. Voltage ripple on the output capacitor during steady state.

Here, the current going through the capacitor is the ac component of the inductor current. The slope of the current in steady state can easily be obtained from circuit analysis

$$S_n^{'} = \frac{V_{in} - V_o}{L}, S_f^{'} = \frac{V_o}{L} \quad (1)$$

where S_n' (S_f') is the inductor current slope during on-time (off-time). The voltage ripple components are summarized in Table 1.

TABLE I. OUTPUT VOLTAGE RIPPLE

	On-time	*Off-time*
v_{ESR}	$ESR \cdot \left(S_n^{'} t - \frac{\Delta i_L}{2} \right)$	$ESR \cdot \left(- S_f^{'} t + \frac{\Delta i_L}{2} \right)$
v_{ESL}	$ESL \cdot S_n^{'}$	$- ESL \cdot S_f^{'}$
v_C	$\frac{S_n^{'}}{2C} t^2 - \frac{\Delta i_L}{2C} t$	$- \frac{S_f^{'}}{2C} t^2 + \frac{\Delta i_L}{2C} t$

The voltage ripple across the ESR of the output capacitor is proportional to the ac component of the inductor current. If the capacitor is large and its ESR is significant, the ripple on the capacitor and the ESL can be neglected. The voltage across the ESR is the dominate part of the output voltage ripple and can be treated as current feedback to the controller. In such a case, a current-mode control method can be applied through sensing the instantaneous output voltage of the capacitor. Only through sensing output voltage gaining both the capacitor voltage and inductor current (i.e. two state variables of the second-order system) feedback is the advantage of V^2 control [11]. Fig. 3 shows a digital V^2 control structure. The output voltage carrying the inductor current information is sensed and converted to a digital representation through an A/D converter. The instantaneous value is directly fed back to the PWM modulator through the inner loop without any low pass filter or compensation, so that a fast transient response can be achieved. The main purpose of the outer loop compensator is to compensate the steady state error.

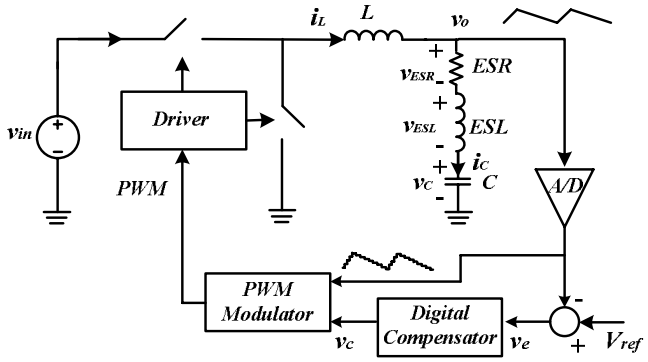

Figure 3. Digital V^2 control for a buck converter.

This paper targets for point-of-load (POL) applications, in which the duty cycle of a buck converter is usually less than 0.5, i.e. the down-slope of voltage ripple is smaller than up-slope in the single phase case. Therefore, it is more desirable to fix the switch on-time, while modulating the off-time. This is particularly true for a digital controller, in which the sampling rate is low. Fig. 4 shows the waveform when digital current-mode constant on-time control is applied to a buck converter. During the steady-state, the output voltage may oscillate due to the limited sampling rate, but the oscillation amplitude is restricted to

$$V_{\text{osc,max}} = S_f \cdot T_{sample} \quad (2)$$

according to the analysis presented in [10], where S_f is the slope of output voltage during off-time and T_{sample} is the sampling period of the A/D converter. Increasing the sampling frequency seems helpful to further reduce the oscillation, but it is not preferred due to higher cost and more power dissipation.

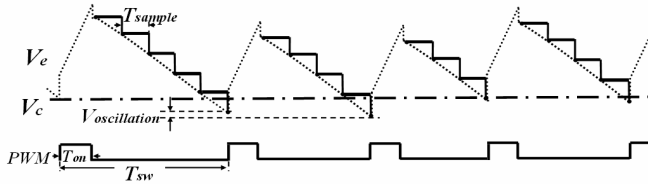

Figure 4. Voltage oscillation in digital constant on-time control.

III. OFF-TIME PREDICTION

When the voltage slope in a constant on-time control is obtained from finite samples within one switching period, the off-time can be calculated and applied to modulate the duty cycle. This is the key idea adopted for the proposed method. We calculate the output voltage slope using two consecutive sampled voltages. The slope $S_f(n)$ at the nth sampled voltage is obtained as follows.

$$S_f[n] = \frac{V_e[n-1] - V_e[n]}{\frac{T_{sample}}{T_{clock}}} \text{ V/cycle}, n = 2, 3, \ldots \quad (3)$$

where $V_e[n]$ is the nth sampled output voltage, $V_e[n\text{-}1]$ is the previous one, T_{clock} is the system clock. For simplicity, we assume that the quantization error of the A/D converter is very small and will discuss it later. The remaining off-time can be calculated by applying the simple tangent function in the triangle shadowed in Fig. 5.

$$T_{remain}[n] = \frac{V_e[n] - V_c}{S_f[n]} \text{ cycle}, n = 2, 3, \ldots \quad (4)$$

where V_c is the control signal obtained from the outer loop compensator, $T_{remain}[n]$ is the predicted remaining off-time at the nth sample. When the remaining off-time decreases to zero or the sampled output voltage is smaller than V_c, the PWM signal goes high to turn on the switch.

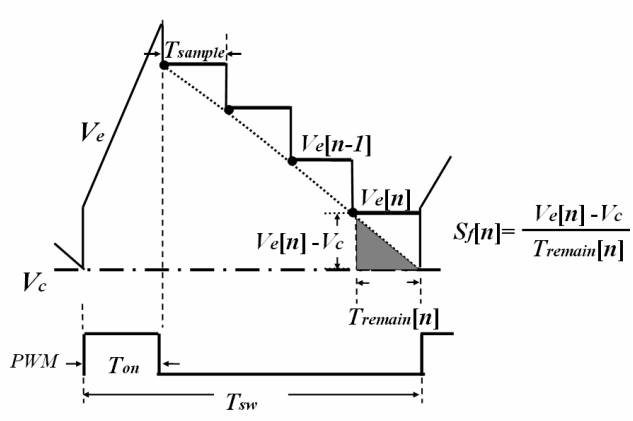

Figure 5. Remaining off-time calculation.

Because the amount of voltage drop in one clock cycle is obtained, the total off-time will be a multiple of system clock periods. Fig. 6 shows an example with T_{sample}=6T_{clock}. The total off-time when applying the prediction method could be T_{off} = 3T_{sample} + 4T_{clock} = 3T_{sample} + 2/3T_{sample}. The total off-time can be a fraction of sampling period; therefore the steady-state oscillation amplitude is not restricted by sampling period as mentioned in (2). Instead of increasing the sampling rate, the off-time prediction method provides another solution to reduce the voltage oscillation amplitude.

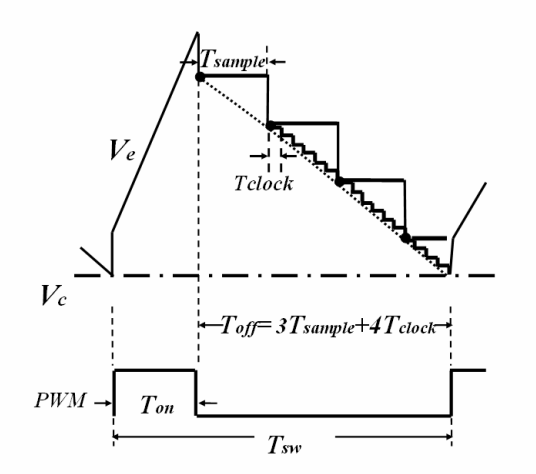

Figure 6. Improvement to oscillation amplitude reduction.

The analysis shown above is based on the assumption of an ideal A/D converter with zero quantization error. For a practical A/D converter with a finite resolution ΔV_{ADC}, it should be able to detect the voltage drop between two consecutive samples. The requirement can be stated as

$$\Delta V_{ADC} < S_f \cdot T_{sample} = ESR \cdot S_f' T_{sample}. \quad (5)$$

If it is not satisfied, the prediction method cannot give precise off-time and may drive the circuit unstable. Considering the output voltage is well regulated to the reference with tight tolerance, the windowed ADCs [2-3] can be used to relax the requirement for high resolution.

The current slope is obtained directly from sampling the output voltage. Therefore, it is not necessary to know the value of the circuit parameters and this control scheme is adaptive to the operating condition of a buck converter such as input perturbation and replacement of analog parts. Furthermore, it does not require an external ramp, the PWM modulation gain F_m is determined by the current slope alone as stated below.

$$F_m = \frac{1}{S_f \cdot T_{sw}} \quad (6)$$

Therefore the dynamic performance does not suffer.

Finally, the ESR of some types of capacitors such as ceramic capacitors is small and results in small S_f. In such a case, it is difficult to extract the current information from the output voltage. It is necessary to adopt other sensing mechanisms such as current transformer or DCR sensing.

IV. EEPERIMENTAL RESULTS

We performed the system simulation of the proposed off-time prediction method with MATLAB and prototyped the system with a buck converter power stage, Xilinx Spartan II FPGA and an external 8-bit A/D converter. The power stage uses inductor L = 300 nH; 8 SP (Single Plate) capacitors (with 390 μF/18 mΩ). We set the input voltage V_{in} = 12 V, the

reference voltage V_{ref} = 1.2 V, input range of the A/D converter is set to be 1.1V to 1.3V. The constant on-time T_{on} = 0.33 μs, the switching frequency T_{sw} ≈ 300 KHz and the system clock frequency f_{clock} = 150 MHz. The A/D converter resolution ΔV_{ADC} = 0.78 mV and sampling frequency f_{sample} = 2.3 MHz (about 8 times of the switching frequency).

The simulation and experimental results for the steady state are shown in Fig.7 and the transient response in Fig. 8. The transient response is the case when the load current has 20 amperes step-up and step-down.

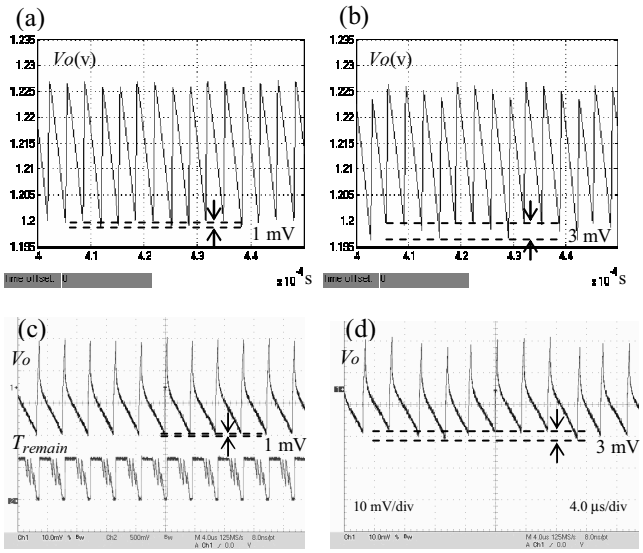

Figure 7. Steady state comparison: (a) simulation with off-time prediction; (b) simulation without off-time prediction; (c) experimental result with off-time prediction ; (d) experimental result without off-time prediction.

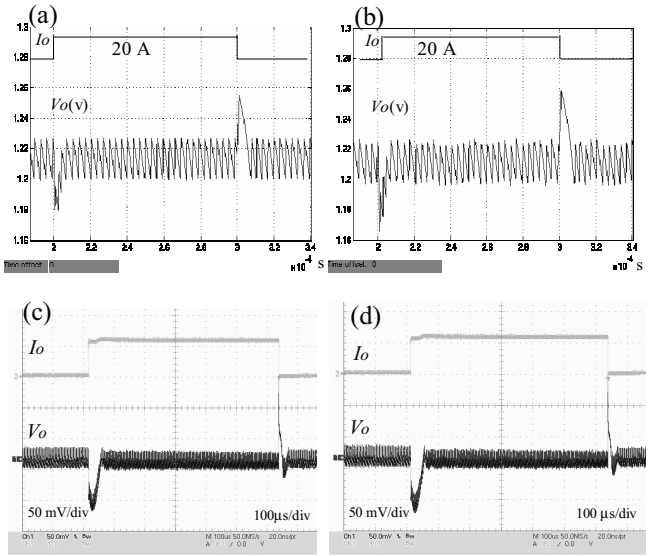

Figure 8. Transient response: (a) simulation with off-time prediction; (b) simulation without off-time prediction; (c) experimental result with off-time prediction; (d) experimental result without off-time prediction.

Fig. 7(c) shows how the prediction method determines the time to turn on the top switch. The prediction method will skip several samples at the beginning of the off-time. After that, the remaining off-time is updated when a new sample is obtained. The value will be stored in a register and decrease at the rate of one per clock cycle. If the value reduces to zero or the sampled output voltage is smaller than V_c, the top switch will turn on.

Both the simulation and the experimental results show that the oscillation amplitude of the output voltage during steady-state is reduced because of the proposed method. Minimum off-time (~1.2 μs) defined in the experiments slows down the recovery from load step-up transient. But compared to without off-time prediction case, the transient response does not suffer.

V. Conclusion

In this paper, an off-time prediction method in digital current-mode constant on-time controller is proposed to reduce the oscillation amplitude of a DC-DC buck converter. This method relaxes the need for high resolution DPWMs and high throughput A/D converters. Both the simulation and the experimental results indicate that the proposed method reduces the oscillation amplitude of the output voltage during steady state while still provides fast transient response.

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