A Feasibility Study on Frequency Domain ADC for Impulse-UWB Receivers

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Abstract— **A feasibility study of frequency domain ADCs for an Impulse-UWB receiver is presented. A frequency domain ADC consists of a bank of narrow band bandpass filters and integrators, followed by a conventional ADC. The filter bank produces the 'spectrum samples' (Fourier series coefficients) at frequencies corresponding to the center frequencies of the bandpass filters in the filter bank. The Fourier series coefficients are sampled and quantized by a conventional time domain ADC. In the baseband of the I-UWB receiver, the digitized Fourier series coefficients can be processed in the frequency domain or the pulse can be reconstructed and processed in the time domain. Sampling in the frequency domain, avoids the need for an ADC with a wide bandwidth and a high sampling rate for an I-UWB receiver. Simulation results on a mathematical model of a frequency domain ADC show that spacing the center frequencies of the bandpass filters at 200 MHz over the band of interest leads to a pulse reconstruction error of ~ 10% for a 5-bit ADC. Practical implementation issues in integrated circuit realization of the frequency domain ADC are described as well.**

Index Terms— ADC, Filter bank, Impulse UWB, Receiver Architectures

I. INTRODUCTION

When compared to the traditional narrow band communication systems, ultra wideband (UWB) technology has several advantages such as high data rate, low-radiated power, excellent immunity to multipaths, and simple hardware. UWB suits many applications such as wireless home networking, sensor network communications, and through-the-walls sensing. Realization of UWB systems in CMOS technology is highly desirable for most UWB applications, but it poses a great challenge for VLSI designers. There are two main flavors of UWB systems, carrier-based (MB-OFDM and DS-CDMA) and impulse-based (I-UWB).

Integrated circuit realization of I-UWB transceivers in CMOS places extremely high requirements on the RF front end and the data converters [1]. The challenge stems from the fact that I-UWB is based on extremely narrow pulses which require high-speed and wide bandwidth circuits for sampling and reconstruction of extremely narrow pulses. Existing CMOS analog-to-digital converters (ADCs) cannot meet the sampling rate necessary for sampling of these UWB pulses. In addition to the high sampling rate, timing jitter makes precise control of sampling time intractable. Many different techniques have been proposed for implementing high speed ADCs viz. the time-interleaved ADCs [2], using bandpass filters to divide the band of interest into several sub-bands and digitizing signals in the sub bands [3]. To ease the requirements on the ADC, analog to digital conversion in the frequency domain has been proposed by the author's group [4] [5] first and then by Hoyos et. al [6] [7], independently.

Although, there are some parallels with our approach and the approach proposed in [6], the hardware implementations are vastly different. The method proposed in [6] uses mixers followed by integrators. The method requires several clock generators, is power hungry and also has noise issues. In our approach, we use narrow band bandpass filters and integrators to extract the Fourier series coefficients at frequencies corresponding to the center frequencies of the bandpass filters. The extracted Fourier series coefficients are digitized using an ADC for further digital signal processing. The digitized Fourier series coefficients then can be processed in the frequency domain or the signal can be reconstructed in the time domain by performing an Inverse Fast Fourier Transform (IFFT) on the Fourier series coefficients and then processed in the time domain. Instead of mixers and multiple clock generators, adoption of filters makes our architecture highly suitable for integrated implementations of I-UWB transceivers. The sampling rate of the conventional ADC employed in the frequency domain ADC is independent of the frequency content of the impulse used for modulating the data and is limited only by the data rate and the number of bandpass filters. In this work, we explore the tradeoffs between the number of bandpass filters and the resolution of the ADC through simulations. Some of practical implementation issues of the filter banks in integrated circuits are also discussed.

The rest of the paper is organized as follows. Section II reviews signal analysis in the frequency domain and the overall architecture of the frequency domain ADC. Section III describes the simulation study of the frequency domain ADC. The trade-offs between the number of filters and the resolution of the time-domain ADC are studied by calculating the pulse reconstruction error. Section IV discusses practical issues in implementing the frequency domain ADC. Section V concludes the paper.

II. PRELIMINARIES

This section reviews the theory behind extraction of Fourier series coefficients from the time domain signals using bandpass filters and the architecture of the frequency domain ADC.

A. Signal Analysis in the Frequency Domain

A continuous time periodic signal with a period Tp can be expressed as

$$x(t) = \sum_{k=-\infty}^{k=+\infty} c_k e^{j2\pi k F_0 t} \qquad (1)$$

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$$c_k = \frac{1}{T_p}\int_{T_p} x(t)e^{-j2\pi kF_0 t}dt \qquad (2)$$

where F0 = 1/Tp is the fundamental frequency of the signal x(t), and a Fourier series coefficient ck represents the spectral component of the signal [8]. Note that ck's are usually complex values, and ck and c-k are complex conjugate. The period Tp is the observation window of the received signal, which is often a fraction of the data rate or Pulse Repetition Interval (PRI). Observe that ck's can be calculated by multiplying the time domain signals with sinusoidal signals and integrating the result over a time period Tp. Direct implementation of (2) requires multiple clock generators, mixers and integrators as shown in [6][7].

Noting that $\omega_0 = 2\pi F_0 = \frac{2\pi}{T_p}$ and using the periodic characteristics of a sinusoidal function, (2) leads to the relation given in (3).

$$c_k = \frac{1}{T_p}\left[\int_{T_p} x(t)\cos(k\omega_0 t)dt - j\int_{T_p} x(t)\sin(k\omega_0 t)dt\right]$$

$$c_k = \frac{1}{T_p}\left[\int_{T_p} x(\tau)\cos(k\omega_0 (T_p-\tau)d\tau - j\int_{T_p} x(\tau)\sin(k\omega_0 (T_p-\tau)d\tau\right]$$

$$c_k = \frac{1}{T_p}\left[x(t) * \cos(k\omega_0 t) + jx(t) * \sin(k\omega_0 t)\Big|_{t=T_p}\right] \qquad (3)$$

where k is integer and '*' is the convolution operation. Noting,

$$L\{\cos(k\omega_0 t)\} = \frac{s}{s^2+(k\omega_0)^2}\ ,\quad L\{\sin(k\omega_0 t)\} = \frac{k\omega_0}{s^2+(k\omega_0)^2}$$

Where $L\{\ \}$ represents the Laplace transform of *x(t)*. (3) can be expressed as following.

$$c_k = \frac{1}{T_p}\left(\left[L^{-1}\left\{X(s)\frac{s}{s^2+(k\omega_0)^2}\right\} + jL^{-1}\left\{X(s)\frac{s}{s^2+(k\omega_0)^2}\right\}\right]\Bigg|_{t=T_p}\right) \qquad (4)$$

where *X(s)* is the Laplace transform of *x(t)*. Our proposed implementation of frequency domain ADC which calculates and quantizes c_k's is based on (4).

Fig. 1 shows (4) in a block diagram form. The block representing the transfer function $\frac{s}{s^2+(k\omega_0)^2}$ can be thought of as a narrow band bandpass filter by observing that the transfer function of a bandpass filter is represented by $\frac{s}{s^2+\left(\frac{k\omega_0}{Q}\right)s+(k\omega_0)^2}$ [9]. Where the parameter Q is defined as in (5)

$$Q = \frac{k\omega_0}{\Delta\omega_{3dB}} \qquad (5)$$

where $k\omega_0$ is the center frequency of the bandpass filter and $\Delta\omega_{3dB}$ is the bandwidth of the filter. The term 'Q factor' often occurs in filter specifications as it defines the relationship of filter's bandwidth to its center frequency. It can be noted that as the bandwidth goes down and the center frequency $k\omega_0$ increases, Q factor increases. Extremely narrow bandwidth filters are sometimes called 'infinite Q' filters [12]. We'll follow similar terminology in the rest of the paper. The block with the transfer function $\frac{k\omega_0}{s}$ represents an ideal integrator, with a pole at DC.

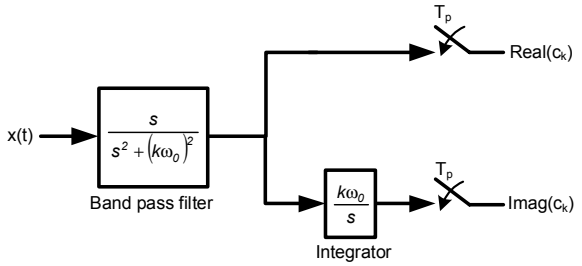


Figure 1: Fourier series coefficient sampler

The output of the 'infinite Q' bandpass filter sampled at Tp gives the real part of the Fourier series coefficient ck. The output of the 'infinite' Q bandpass filter integrated by an ideal integrator with a gain of $k\omega_0$ and sampled at Tp gives the imaginary part of the Fourier series coefficient ck. Implications for realization of these blocks in integrated circuits will be discussed in section IV.

B. Frequency Domain ADC

Consider a train of pulses at a receiver as shown in Figure 2. Our goal is to obtain sampled values of the individual pulses using an ADC. Let τ0 be the observation window of each pulse and T is the PRI. Assume that pulses require over-sampling by a factor of N. The conventional method, which over-samples a pulse by factor of N during τ0 with a single ADC, requires the ADC to sample at a rate of N/τ0. For example, the sampling rate is an impractical 32 GHz for N=8 and τ0 = 250 ps.

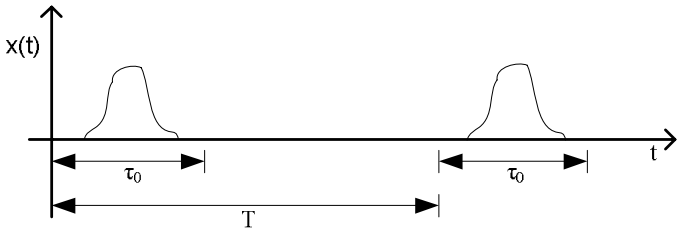


Fig. 2: Received input pulses

The architecture of the frequency domain ADC is given in Fig. 3. The received signal x(t) is applied to a bank of filter structures shown in Fig. 1. The center frequencies of the 'infinite Q' bandpass filters are spaced equally within the band of interest used for I-UWB communications. The filter bank outputs the Fourier series coefficients ck's corresponding to the center frequencies of the bandpass filters. The output of the filters are sampled at the end of the observation period τ0. A single ADC sweeps through the filter back outputs from 2*N sample and holds once every T seconds, where N is the number of filters in the filter bank and T is the PRI. Sampled Fourier series coefficients are then digitized by a conventional ADC. The digitized fourier series coefficients can be processed in the

frequency domain for a fully frequency domain I-UWB receiver or the original pulse can be reconstructed by performing IFFT on the Fourier series coefficients and then the time domain samples of the pulse can be processed.

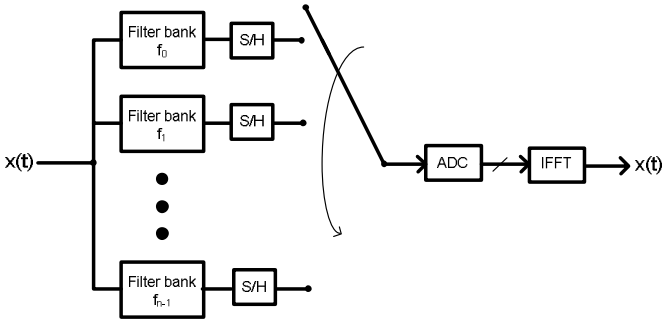


Fig. 3: Frequency domain ADC architecture

III. Simulation Results with Ideal Filter Banks

This section describes the simulation setup for evaluation of our frequency domain ADC and impact of the number of filters and the ADC resolution on the pulse reconstruction.

A. Simulation Setup

In order to verify the performance of the frequency domain ADC, we modeled equation (4) in Matlab. The input pulse was a Gaussian mono-pulse. The lower band of UWB communications (3 - 5 GHz band) was chosen for simulations. The pulse was band-limited to 3-5 GHz with a 128-tap Ramez digital filter. The band-limited pulse was normalized to have a Vp-p of 1 V and is shown in Fig. 4.

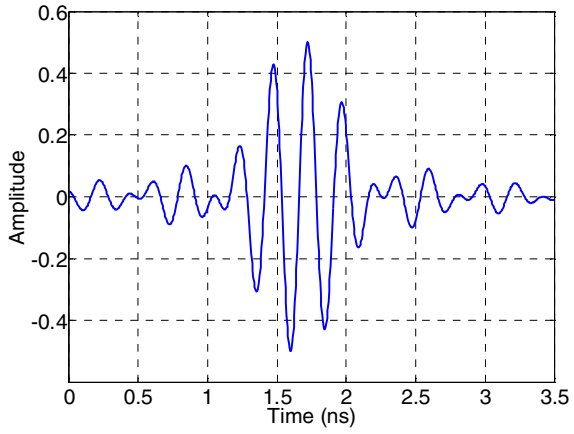


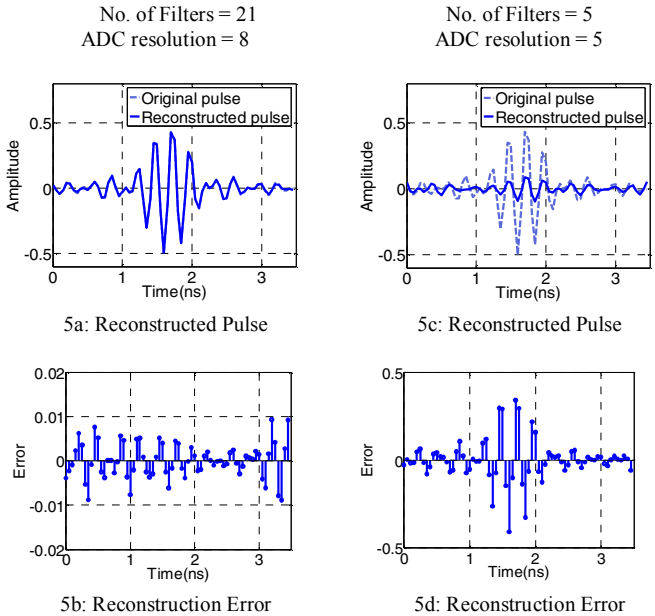
Fig. 4: Band-limited pulse (3-5 GHz band)

The center frequency of the bandpass filters was spaced equally in the 3-5 GHz band. The number of filters for corresponding frequency spacing in the 3-5 GHz band is shown in Table I. For example, a frequency spacing of 100 MHz in the 3-5 GHz band corresponds to 2 GHz/100 MHz +1 = 21 filters because the frequencies at the band edges viz. 3 GHz and 5 GHz have to be covered as well. The spectral components corresponding to other frequencies are filled with zeroes to reconstruct the entire spectrum with the effective target sampling rate of 20 GHz. The effective sampling rate can be increased (decreased) by increasing (decreasing) the number of zeros. For example, consider 500 MHz frequency spacing with 5 filter banks. To meet a target sampling rate of 20 GHz, 21 samples (10GHz/500MHz + 1) are required to reconstruct the frequency spectrum from DC (0 Hz) to half the sampling rate (10 GHz). Thus, 5 zeros are inserted to cover the spectrum from 0 to 2.5 GHz followed by 5 frequency samples obtained from the frequency domain ADC in the band from 3 GHz to 5 GHz and then 11 zeros are inserted to cover the spectrum from 5.5 GHz to 10 GHz.

TABLE I. Number of Filters Vs. Frequency Spacing

Frequency Spacing (MHz)	Number of Filter Banks
500	5
400	6
300	7
200	11
100	21

The frequency spectrum samples or the Fourier series coefficients output by the filter bank are then digitized by an ADC modeled in Matlab. The IFFT operation is performed on the quantized spectrum samples and the reconstructed frequency spectrum. The pulse and reconstruction error are illustrated in Fig. 5 for two different combinations of number of filters and ADC resolutions.



5a: Reconstructed Pulse

5c: Reconstructed Pulse

5b: Reconstruction Error

5d: Reconstruction Error

Fig. 5: Reconstructed pulse and error

The reconstructed pulse is shown in Fig. 5a when the filter bank had 21 filters and the ADC resolution was 8. The error between the original pulse and the reconstructed pulse is shown in Fig. 5b. From the two figures, one can observe that this case corresponds to the near-perfect reconstruction with the maximum reconstruction error being less than 0.01. The reconstruction error increases as the number of filters is

decreased and as the resolution of the ADC is decreased. Figure 5c shows the reconstructed pulse for 5 filters and ADC resolution of 5 bits. The reconstructed pulse in this case deviates largely from the original pulse and the maximum reconstruction error is 0.4 for an input pulse with Vp-p of 1.

In order to quantify the reconstruction error, we defined a parameter called the RMS Error Percentage (RMSEP) given by (6).

$$RMSEP = \frac{RMS(\text{Original Pulse} - \text{Reconstructed Pulse})}{V_{pp} \text{ of Orginal Pulse}} x100\% \qquad (6)$$

B. *Impact of number of filters and the ADC resolution*

The variation of the RMSEP for different number of filters and the ADC resolution is shown in Fig. 6. The number of filters is determined by the frequency spacing of the center frequencies of the bandpass filters (ΔF). The reconstruction error curves for different numbers of filters follows the similar trend. As the number of filters decreases, the error percentage increases. The biggest increase is observed when the frequency spacing is changed form 100 MHz to 200 MHz. Note that in this case, the number of filters is halved from 21 to 11. The increase in error percentage is more gradual as the number of filters is decreased and as the spacing between center frequencies of filters is increased.

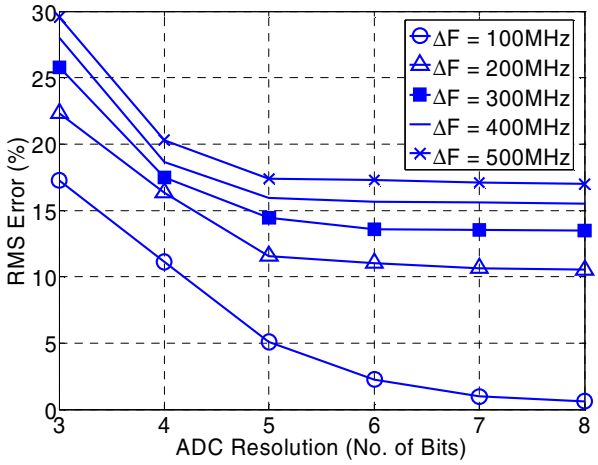


Fig. 6: Reconstruction Error vs. ADC resolution

An interesting trend observed is that the RMSEP pretty much saturates around 5 bits of ADC resolution except for the case when ΔF = 100 MHz. Therefore, we conclude that an ADC resolution of 5 bits is sufficient for minimum reconstruction error from the frequency domain ADC. Also, we noted in section 2.2, that the sampling rate of this conventional ADC is only a fraction of the PRI (determined by the number of filters to be sampled). For example, for a PRI of 50 ns and 11 filters, the sampling rate for the conventional ADC is $\frac{2\times11}{50\times10^{-9}} = 440$ MHz, which is easily realizable with current CMOS technologies. Further, a 5-bit, 440 MHz ADC will only consume a small fraction of the overall frequency domain ADC's power.

For the case when ΔF = 100 MHz, the error percentage decreases significantly as the ADC resolution increases and saturates around 7 bits. However, when ΔF = 100 MHz, we need 21 filters and RMSEP of the order of 2% corresponds to near perfect reconstruction as shown in Fig. 5a which may not be required in every application. We conclude that an optimal filter spacing would be ΔF = 200 MHz (11 filters for our band of interest) and an ADC resolution of 5 bits.

IV. Practical Filter Bank Design Issues

A practical implementation of the filter structure given in Fig. 1 is shown in Fig. 7. The 'infinite Q' bandpass filter shown in Fig. 1 is replaced by a conventional bandpass filter with the transfer function $\frac{s}{s^2+\left(\frac{k\omega_0}{Q}\right)s+(k\omega_0)^2}$, but Q in this case is assumed to be very high. So that, the overall transfer function tends to be $\frac{s}{s^2+(k\omega_0)^2}$ as in Fig. 1. Filter structures for implementing infinite Q filters have been studied nearly two decades ago [12] and these structures can be used for implementing infinite Q filters without having to reinvent the wheel. Implementing, an ideally 'infinite Q' filters has practical limitations, however, these structures can readily achieve very high Q factors (of the order of 200~300). Since the unity gain frequency (f_T) of the current CMOS technologies are in the order of 200 GHz [13], bandpass filters with center frequencies in the GHz range can be easily realized. In order to counter the extreme process variations in deep submicron technologies, the filter center frequency and the bandwidth must be tunable.

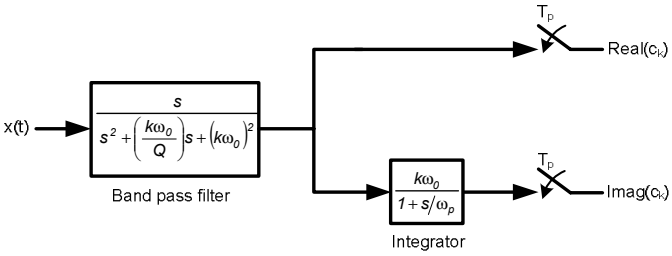


Fig. 7: Practical implementation of a Fourier series coefficient sampler

The ideal integrator $\frac{k\omega_0}{s}$ in Fig. 1 is replaced with a practical integrator $\frac{k\omega_0}{1+s/\omega_p}$. A pole at DC would require infinite output impedance. However, output impedances in the order of MΩs can be obtained with current CMOS technologies operating at very low voltages through cascoding or gain-boosting techniques [14]. The gain in the numerator $k\omega_0$ corresponds to the center frequency of the bandpass filter. For our case, since the band of interest is from 3 to 5 GHz, the required amplifier gain will also be in this range i.e. 3 x 10^9– 5 x10^9. Open loop gains of CMOS op-amps are usually in the range of 10^5 [15] so the gains of this range can be obtained by cascading open loop op-amps. The main issue is to maintain the stability of the amplifier when operating at such high gains as well as the variability of the gain. Again, some tunability should be

introduced into the integrator gain, to counter the process variations.

V. CONCLUSION

A simulation study of the frequency domain ADC for sampling I-UWB signals is presented. For the simulation study, the pulse is reconstructed from the spectrum samples and the reconstruction error is calculated. Optimum spacing of the center frequencies of the filter banks and the resolution of the ADC is determined by considering hardware complexity and an acceptable pulse reconstruction error. Although the ideal integrator and 'infinite Q' bandpass filter may not be realizable in practice, circuits that realize 'nearly infinite Q' filters as well as 'nearly ideal' integrators have been investigated previously, and some of these structures can be reused. Based on our simulations and investigation on the practical implementation issues, we conclude that frequency domain sampling ADCs provide a means for processing narrow pulses for I-UWB transceivers without relying on extremely high sampling rates and a large number of bits.

ACKNOWLEDGMENT

This material is based upon work supported by the National Science Foundation under Grant No. 0551652.

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