Design of a Data Recovery Block for Communications over Power Distribution Networks of Microprocessors

Vipul Chawla, Rajesh Thirugnanam
and Dong Sam Ha
VTVT (Virginia Tech VLSI for Telecommunications) Lab
Department of Electrical and Computer Engineering
Virginia Tech, Blacksburg, VA – 24061
Email: {vipulece, thirugnr, ha}@vt.edu

T. M. Mak
Research Scientist
Sort Test Technology Development
Santa Clara, CA - 95054
Email: t.m.mak@intel.com

Abstract: We proposed the use of power distribution network (PDN) of a microprocessor for ubiquitous access of internal nodes for test/debug and showed the suitability of impulse ultra-wideband (UWB) communications for the purpose. This paper presents design of a data recovery block to recover data from UWB impulses superposed on a power line of a microprocessor. Considerations for data recovery block design based upon measured PDN characteristics have been discussed. The proposed circuit was implemented in TSMC 0.18 um CMOS process, and simulations show that it consumes 4.42 mW when operating from a 1.8V supply and at a pulse repetition rate of 200 MHz.

Keywords — Microprocessor; Power line communication; Impulse UWB Receiver; Power distribution network

I. INTRODUCTION

As the complexity of a modern microprocessor increases rapidly and seemingly without bound, testing and debug strategies have to be constantly re-invented in order to keep pace with the complexity. Currently, there exists no systematic method to diagnose a system after it crashes and fails to reboot. Also, it is difficult to continuously monitor so called "large time-constant errors" i.e. errors that creep up over a period of time due to variations in temperature and aging. To support resilient operations in these constantly varying conditions, extensive monitoring is required throughout the entire die. Although self-test circuits are used to estimate these variations on a microprocessor die, most of the test circuits are either removed once the chip is deployed on the field or offer very limited access.

The power distribution network (PDN) is ubiquitous across a microprocessor, i.e., a power line is accessible to any internal node. If a power line can be used to communicate with the external world, it can avoid preplanned routing of a data path from a node to an external data pin. This is a highly attractive feature for testing, as the routing of data paths is expensive in design time as well as in silicon area. The ability to monitor internal node values without routing data paths opens up a possibility for fault diagnosis, monitoring transient logic values during built-in self test, sending control data to sensors, and for on-line testing.

Power line communications (PLC), patented in the early 1920's, has been mainly considered by utility companies for remote metering and control [1]-[2]. Recently, it has been revived for broadband internet access over existing power lines [3]. The use of power lines in an IC environment was introduced by the authors' group in [4] and extended to massive scan chains in [5]. As noted in [4]-[5], PLC in a microprocessor faces a totally different set of technical challenges from that of traditional PLC as described below. Most importantly, the noise characteristics as well as the communication channel of the power distribution network are completely different from a traditional PLC. The power distribution network is very noisy due to the so called IR drop, Ldi/dt, and thermal noise [6]. Second, the signal power level at a power distribution network should be sufficiently small not to disturb the correct operation of the circuit, which makes the recovery of data from a noisy power line difficult. Note that such noise is not a major problem for traditional PLC. Finally, a microprocessor PDN is heavily decoupled to filter out the low frequency power supply noise as well as reduce the slew rate of current variations by locally supplying currents to switching nodes. Consequently, the PDN looks like a bulky lowpass filter for high frequency signals. However, it is well known that the inductance component of decoupling capacitors becomes significant beyond the self resonant frequency of the capacitors. This range band of frequencies can be used for communication using impulse ultra wideband (UWB).

The rest of the paper is organized as follows. Section II describes the impulse UWB signaling over a microprocessor PDN, overall architecture of the PLC, and design considerations for the data recovery block. Section III describes the circuit-level implementation of the data recovery block. Section IV describes the performance evaluation of the proposed data recovery block and section V concludes the paper.

II. PRELIMINARIES

This section describes signaling and modulation schemes for PLC, the overall architecture of the proposed power line communication method, measured PDN characteristics and its implications on system design.

A. Overall Architecture and Modulation Scheme for PLC

Compared to traditional narrowband communication systems, UWB has several advantages such as high data rate, low average power, and simple RF circuitry. Shannon's theorem states that the channel capacity C is given as $B \times \log2(1+SNR)$ [7], where B is the bandwidth and SNR is signal-to-noise ratio. As the bandwidth B is much larger (on

978-1-4244-1708-7/08/$25.00 ©2008 IEEE

the order of several GHz) for UWB than for a narrowband signal, the SNR can be much smaller for UWB to achieve the same data rate. Therefore, with UWB communications one can often recover data, even if the signal power is close to the noise level. In other words, the power level of UWB signals can be at the noise level of power lines to have little impact to the power integrity.

UWB signaling can be carrier-based or impulse-based. Impulse UWB is more suitable for the proposed application due to its simple hardware [8]. Impulse UWB is based on a train of narrow pulses (which are typically a few hundreds picoseconds wide). The most popular pulse shapes used for impulse UWB are Gaussian pulses and their derivatives [8]. Various modulation schemes such as On-Off Keying (OOK), Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM) and Binary Phase Shift Keying (BPSK) are available for UWB. We adopt BPSK for sending data to the internal nodes due to its efficient performance and simple implementation. In this modulation scheme, the two possible bit values are represented by positive and negative pulses.

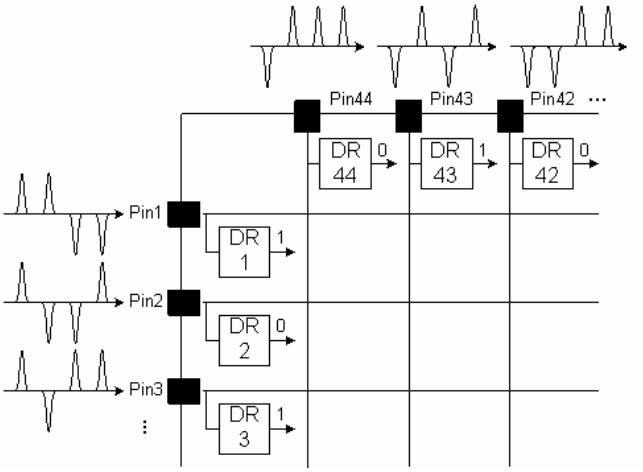

Figure 1: Simplified overall architecture

A simplified overall architecture of the proposed PLC is shown in Figure 1. The architecture does not show power and ground planes for brevity. The impulse modulated data to be sent over the PDN can be applied on any of the power pins. The data recovery (DR) blocks are located at various internal nodes. In addition to sending control data to a single sensor, different data can be sent to different sensors simultaneously using multiple access techniques borrowed from wireless communications, preferably Direct Sequence Code Division Multiple Access (DS-CDMA), so as to keep the data recovery digital and simple.

B. Measured PDN Characteristics and its Implications on Data Recovery Block Design

The most important requirement for designing a communication system is knowledge on the characteristic of the communication channel. Efforts were made to characterize an Intel microprocessor's PDN channel. The channel characteristic for a 65 nm Pentium processor was measured by our group, and its results were published in [9]. Following the initial measurement, another measurement campaign was conducted on 45 nm Core 2 Duo processors. It was observed through the measurement campaigns that passbands exist for microprocessor PDNs. These pass-bands were mainly observed in the 0 to 3 GHz frequency band as illustrated in Figure 2, where y-axis denotes magnitude of the measured s21 or the power spectral density of a Gaussian impulse (in dB scale). However, the locations of passbands tend to vary not only from one process technology to another, but also from die to die. An effective way to cover passband variations is to use a UWB impulse, which covers the entire band of 0 to 3 GHz as indicated as a dotted line in Figure 2.

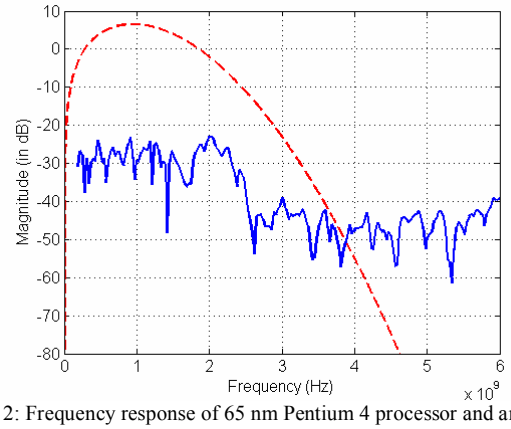

Figure 2: Frequency response of 65 nm Pentium 4 processor and an impulse UWB spectrum

We also observed existence of multi-path signals at an internal node due to different signal paths and reflections from signal boundaries. Among multi-path signals, the first multi-path impulse is the strongest and hence should be captured by a data recovery block. There are several other design requirements for a data recovery block. First, it should be able to detect small variations from its supply voltage. Note that this situation is seldom encountered for other circuit design. Second, a microprocessor PDN is extremely noisy due to the enormous switching activities taking place on the die. Therefore, the circuit should have high noise immunity. Finally, like most other circuits, it should be digital-process friendly with small area and low power dissipation. In other words, the design should use analog circuits and voltage references sparingly.

III. Data Recovery Block Circuit

This section presents the overall architecture of our data recovery block and describes the circuit-level implementation of each sub-block.

A. Overall Architecture

Receivers for impulse UWB are broadly categorized as threshold or leading edge detector, correlation detector, and RAKE receiver. Although a RAKE receiver is more robust, but a leading edge detector and a correlation detector are simpler in implementation. A correlation detector is adopted for our design because it is sensitive to total received power rather than peak power. Note that capturing the maximal signal power is important due to high level of noise on power lines for a microprocessor.

The block diagram of a data recovery block based on correlation detection is shown in Figure 3. The clock triggers a template generator to generate a template signal in synchronous to an incoming impulse. An optimal template for an impulse UWB receiver is one that matches to the received pulse waveform; however, template generation of such waveform is complex and power hungry [10]. Therefore, we adopted a digitally generated Gaussian impulse as a template. The following sub-sections describe the circuit design of each stage of the data recovery block.

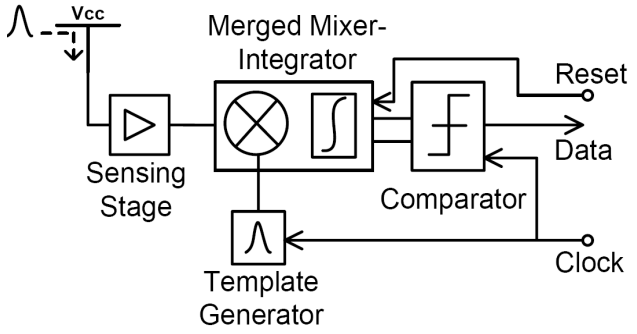

Figure 3: Data recovery block architecture

B. Sensing Stage

A rather unique requirement of our application is to detect short duration perturbations over power line. We proposed a sensing circuit, in which the isolation between the supply voltage and the circuit output is intentionally reduced, i.e. the power supply rejection ratio (PSRR) is weakened artificially [11]. The sensing circuit described here improves upon our earlier design by increasing the gain of the circuit.

Figure 4 shows the sensing stage. The sensing circuit can be seen as a common-gate amplifier with M1 as the input transistor and M2 as the active load. The common-gate configuration inherently has a large bandwidth [12], which is desirable for our application. The sensing stage was designed for a gain of 15 dB at 1.5 GHz and its output DC level was set to 0.5Vdd.

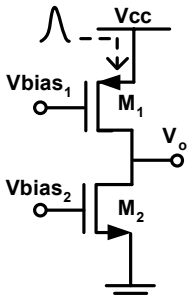

Figure 4: Sensing circuit

C. Template Generator

The template generator is shown in Figure 5. One of the inputs to the NOR gate is inverted and delayed with respect to the other by introducing an odd number of inverters. Every time the clock signal switches from Vdd to 0, a glitch is generated at the output (Vtmp). The generated glitch is the template waveform for the correlation. The glitch duration can be adjusted by controlling the delay between the two inputs of the NOR gate. Therefore, a template is generated at every clock transition from Vdd to 0. The chain of inverters on the clock line delays the clock signal and synchronizes the template with the first impulse received.

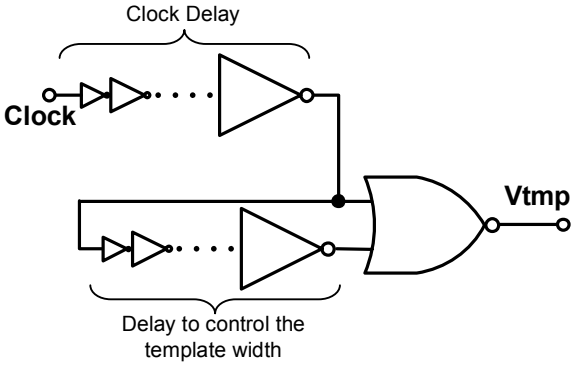

Figure 5: Template generator

D. Merged Mixer-Integrator

The mixing and integration functions have been merged into one circuit using a single-balanced current-mode mixer with capacitive loads as shown in Figure 6. A similar passive mixer was reported in [13]. However, since the observed signal level in our application is much lower, we use an active configuration for additional gain.

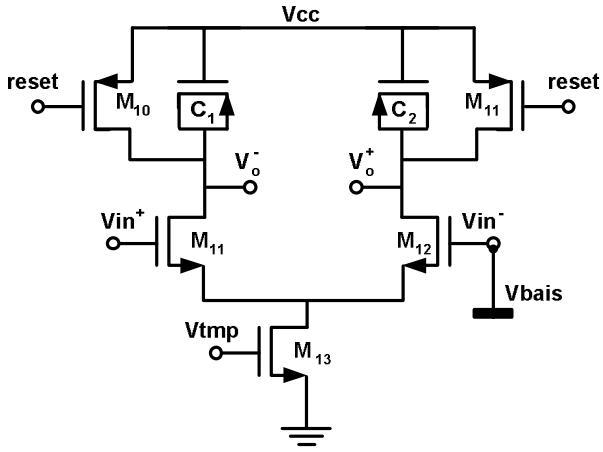

Figure 6: Merged mixer-integrator

The lower half of the circuit is a single-balanced mixer formed by transistor M11, M12 and M13. The output of the sensing stage is connected to M11, while the input of M13 is connected to a fixed bias point (0.5Vdd), equal to the DC output level of the sensing stage. In fact, the bias voltage Vbias2 of the sensing stage is reused for that of M12. The current output of the mixer is integrated using MOS-capacitors C1 and C2 to generate a differential output voltage.

During the high clock period, output voltage V_o^- of the mixer-integrator falls faster (slower) than V_o^+ for a positive (negative) input impulse provided the received and template

waveforms are synchronized. The circuit is reset during the low clock period, which charges both outputs back to the supply voltage level Vdd. The mixer output is regenerated to a digital logic level using a positive feedback latch shown in Figure 7.

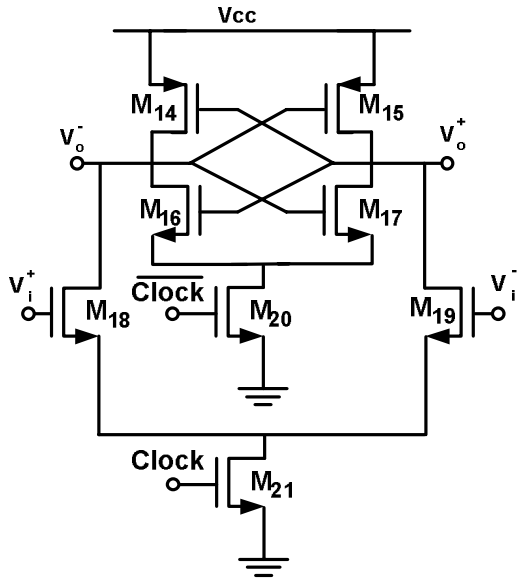

Figure 7: Positive feedback latch

IV. Performance Evaluation

The data recovery block described above was designed and simulated with the target technology of TSMC 0.18 µm CMOS process under supply voltage of 1.8V. Since the supply voltage variation for a microprocessor is typically allowed up to ±5% [14], we set the maximum amplitude of received pulses to 20 mV for our simulation. Note that it is far lower than the maximum allowed supply voltage variation of 90 mV to leave some margin to the supply voltage variation. The pulse-duration was set to 200 ps with a pulse repetition-rate of 200 MHz.

Simulation results for the data recovery block are shown in Figure 8. The top graph shows received impulses at the input of the data recovery block. The second and third graphs are clock and reset signals, respectively. The reset signal of 500 ps duration is activated at the falling edge of the clock. The fourth graph shows differential outputs of the mixer, with an upward (downward) arrow indicating a positive (negative) difference for a positive (negative) pulse. The last plot shows successful recovery of a digital logic value at the falling edge of a clock.

The circuit performance was also evaluated across PVT variations using Mote-Carlo simulations. (The process and mismatch variation parameters were provided by the foundry.) Our Mote-Carlo simulations indicate successful operation of the circuit across 3-sigma worst case process variations.

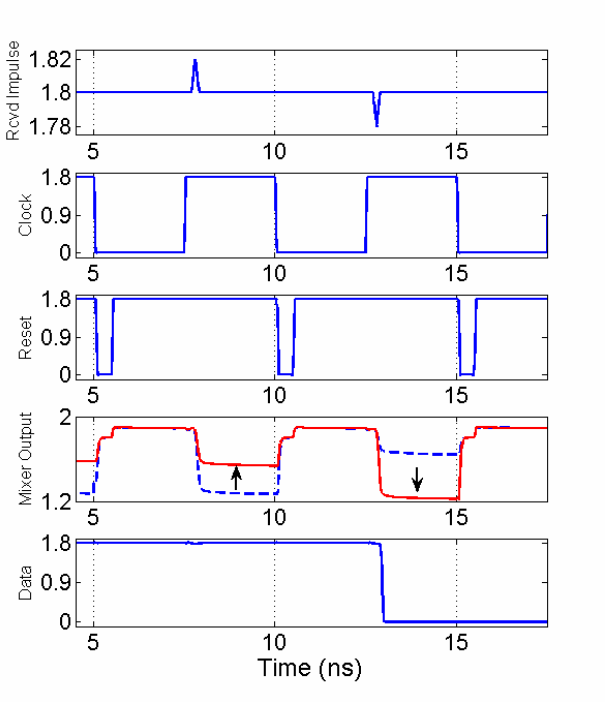

Figure 8: Transient simulation

The performance of data-recovery block is summarized in Table 1.

TABLE 1. PERFORMANCE SUMMARY

Pulse Amplitude	20 mV
Pulse Duration	200 ps
Pulse Repetition Rate	200 Mpps
Sensing Stage Power Consumption	3.78 mW
(Mixer+Latch) Power Consumption	546 µW
(Template Generator) Power Consumption	100 µW
Total Power Consumption	4.42 mW

V. Conclusion

A new scheme was proposed for ubiquitous access of internal nodes of microprocessors for testing/debug. It adopts impulse UWB communications over power distribution networks of microprocessors [4]-[5]. We presented design of a data recovery block based on a simple mixer-integrator operation. Our simulation results indicate that the data recovery block successfully recovers data from UWB pulses superposed on power lines.

References

[1] T.-W. Chan and T.-Y. Lim, "Application of A-Band LV power line standards for remote metering at populous residential buildings", *IEEE/PES Asia Pacific Transmission and Distribution Conference and Exhibition*, Vol. 2, pp. 969 - 974, October 2002.

[2] I.H. Cavdar, "A solution to remote detection of illegal electricity usage via power line communications," *IEEE Transactions on Power Delivery*, Vol. 19, No. 4, pp. 1663-1667, October 2004.

[3] S. Galli, A. Scaglione, and K. Dostert, "Guest Editorial - Broadband is power: Internet access through the power line network," *IEEE Communications Magazine*, Vol. 41, No. 5, pp. 82-83, May 2003.

[4] W. C. Chung, D. S. Ha, and H. J. Lee, 'Dual use of power lines for data communications in a system-on-chip environment,"

Proceedings of IEEE International Symposium on Circuits and Systems, Vol. 4, pp. 3355-3358, May 2005.

[5] W. C. Chung, and D. S. Ha, "A new approach for massive parallel scan design," *Proceedings of IEEE International Test Conference*, pp. 497-506, November 2005.

[6] N.H.E. Weste, and K. Eshraghian, *CMOS VLSI design – a circuit and systems perspective*, 3rd Ed., Addison-Wesley Publishing Co., 2005.

[7] John G. Proakis, "Digital communications," McGraw-Hill Higher Education, 4th Ed. 2000.

[8] J. H. Reed (Editor), "*An introduction to ultra wideband communication systems,*" Prentice Hall, 2005.

[9] R. Thirugnanam, D.S. Ha, and T. M. Mak, "On Channel Modeling for Impulse-Based Communications over a Microprocessor's Power Distribution Network", *International Symposium on Power Line Communications*, pp.355-359, March 2007.

[10] P. Heydari**, "**A study of low-power ultra wideband radio transceiver architectures," *IEEE Wireless Communication and Networking Conference*, pp. 758-763, Match 2005.

[11] R. Thirugnanam, D.S. Ha, and T. M. Mak, "Data Recovery Block Design for Impulse Modulated Power Line Communications in a Microprocessor", *IEEE Computer Society Annual Symposium on VLSI*, pp. 153-158, May 2007.

[12] D. J. Allstot, L. Xiaoyong, S. Shekhar, "Design considerations for CMOS low-noise amplifiers", *Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 97-100, June 2004.

[13] T. Terada, S. Yoshizumi, M. Muqsith, Y. Sanada, T. Kuroda, "A CMOS Ultra-Wideband Impulse Radio Transceiver for 1-Mb/s Data Communications and ±2.5-cm Range Finding", *IEEE Journal of Solid-State Circuits*, pp. 891-898, April 2006.

[14] Q. K. Zhu, "*Power distribution network design for VLSI*", N. J. Hoboken, Wiley-Interscience, 2004.