Automated System Identification of Digitally-Controlled Multi-phase DC-DC Converters

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***Abstract*- Real-time system identification is desirable for designing a proper feedback controller in a practical system. Digital control provides the potential advantages of on-line programmability to apply adaptive control. The digital nature of the feedback signal facilitates the communication between the converter and the processing unit (e. g., microcontroller). These features of digital control make it possible to estimate the real-time system parameters by means of system identification in situ (in-place), and then design and configure the controller accordingly. In this paper, an automated system identification method for digitally-controlled multi-phase DC-DC converters is set forth. Fourier analysis is utilized because of the potential for closed-loop identification and high measurement signal-to-noise ratio. The phase loss and zero-order-hold due to digital control are considered. The identification results for single- and multi-phase DC-DC converters closely match those obtained from conventional network analyzer and models. The proposed method can be done by a stand-alone digital controller; therefore it eliminates the expense of external test equipment. The identification results can be used for controller configuration without pre-existing knowledge of the power stage parameters. This opens up a possibility of moving the determination of the loop compensation from a lab bench to a factory floor or even to an end customer's application.**

***Index Terms*- system identification, digital control, DC-DC converters**

I. INTRODUCTION

Conventional controller design approaches require the knowledge of system parameters and operating conditions [1]. The overall system model of a power module operating in parallel or interacting with other modules might not be predictable [2, 3], necessitating the use of real-time system identification to properly design the feedback controller. Digital control provides the potential advantages of on-line programmability and the application of adaptive control. The digital nature of the feedback signal facilitates the communication between the converter and the processing unit (e. g., microcontroller), allowing us to estimate real-time closed-loop system parameters without the need for external test equipment. This facilitates the measurement of the power system in situ (in-place) such as during factory test or after it is installed in the end application.

System identification can be performed on open- and/or closed-loop converters, although the latter form is generally preferred due to its lower disruption of the system operation. Conventionally, dynamic characterization is estimated injecting an excitation signal and subsequent post-processing of the response (e.g., transient-response [4, 5], correlation analysis [4-6], frequency-response [4, 5], Fourier analysis [4, 5, 7], spectral analysis [4, 5]). The excitation signal is typically an impulse, step, or white noise in time-domain approaches, or a set of sinusoidal waveforms in frequency-domain approaches. Time-domain approaches are not common in closed-loop analysis, since the output will in turn affect the input and excitation and noise signals are then correlated [5]. Therefore, a frequency-domain approach with a sinusoidal perturbation injection and a swept frequency technique is preferred to identify the closed-loop characteristics. This is also the technique used by commercial network analyzers because it provides a high signal to noise ratio (SNR) at a given frequency.

In this paper, an automated system identification method based on closed-loop Fourier analysis for digitally-controlled multi-phase DC-DC converters is described. The proposed methodology is demonstrated on single- and multi-phase DC-DC buck converters. The resulting open- and closed-loop transfer functions are verified by comparing to an average model [1] and a network analyzer.

II. GENERAL THEORY OF AUTOMATED SYSTEM IDENTIFICATION

The theory and guidelines for loop-gain direct measurement are well illustrated in [8, 9]. To save the hardware cost, the indirect measurement of the loop-gain [10] is adopted in this paper. In the closed-loop system shown in Figure 1, $r(n)$ is the excitation signal that is the digital reference for the output voltage $y(t)$ of the power stage. The digital excitation signal is injected to the system at the rate of F_s and converted to analog signal $r(t)$ by a DAC. The error $e(t)$ of output voltage compared to the reference is converted to digital signal $e(n)$ at the rate of F_{sample}. The closed-loop response $u(n)$ is read at the output of digital compensator and converted to analog PWM signal $u(t)$ by digital pulse-width modulator.

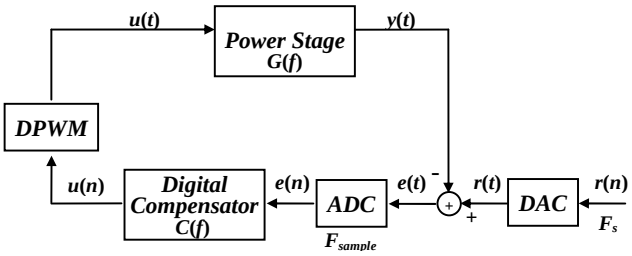

Figure 1. System block diagram of digitally controlled power converters

If the analog-digital interfaces such as DAC, ADC and DPWM are assumed to have a linear gain of one, the closed-loop transfer function from excitation $r(n)$ to response $u(n)$ is

$$T_{cl}(f)=\frac{U(f)}{R(f)}=\frac{C(f)}{1+G(f)\cdot C(f)} \tag{1}$$

where $U(f)$ and $R(f)$ are the discrete Fourier transform (DFT) of the response and reference signals, respectively, and $G(f)$ and $C(f)$ are the control-to-output transfer function and the compensator's transfer function, respectively. For a sinusoidal excitation sequence $r(n)$ with the frequency of f_i, the DFT complex coefficient for the single frequency is calculated as

$$\begin{aligned} R(f_i)&=\sum_{n=0}^{N-1} r(n)\cdot e^{-j2\pi\frac{f_i}{F_s}n} \\ &=\sum_{n=0}^{N-1}\left(r(n)\cdot\cos\left(2\pi\frac{f_i}{F_s}n\right)\right)-j\cdot\sum_{n=0}^{N-1}\left(r(n)\cdot\sin\left(2\pi\frac{f_i}{F_s}n\right)\right) \end{aligned} \tag{2}$$

where N is the length of the injection sequence and F_s is the injection frequency at which the sine wave is injected. Likewise, the DFT complex coefficient of the excitation frequency f_i, i.e. $U(f_i)$, is calculated for the response signal. By sweeping the frequency of sinusoidal excitation signal in the frequency range of interest, the control-to-output transfer function can be obtained as

$$G(f)=\frac{1}{T_{cl}(f)}-\frac{1}{C(f)}=\frac{R(f)}{U(f)}-\frac{1}{C(f)} \tag{3}$$

The above algorithm is based on the assumption of a time-invariant linear system. Unfortunately, a digitally controlled power converter has inherent nonlinearity due to the quantization of the error signal and control effort in the feedback loop. The nonlinear effect is more pronounced when the amplitude of quantizer input signal is less than one least-significant-bit (LSB), and the nonlinear gain of the quantizer is also a function of the input's offset to the quantization levels [11]. In this paper, efforts have been made to identify the power stage at a specific operating point which can be treated as a linear system with a designated perturbation to make the closed-loop system react linearly. The amplitude of input signal is set to be greater than two LSBs, which is large enough to force the quantization gain to be near unity. At the same time, the amplitude is also small enough to avoid disturbing the normal operation point.

A careful examination of the digital control feedback loop reveals that there are two contributors to phase delay in the system that need to be considered. As shown in Figure 2, for a trailing-edge modulator, the first is a delay denoted as T_{delay1} from the moment that the output voltage is sampled to the time the calculated control effort is applied to the system. The sampling instance can be programmed in the firmware to be as close as possible to the rising edge of PWM to minimize T_{delay1}. Another delay is denoted as T_{delay2} and is from the moment that control effort is calculated to the time at which it is applied to the system at the falling edge of PWM pulse [12]. For a multi-phase converter, T_{delay2} is the summation of average on-time and average delay given in (4).

$$\begin{aligned} T_{delay2}&=\frac{1}{N_{phase}}\sum_{n=1}^{N_{phase}}T_{phase,n} \\ &=D\cdot T_{sw}+\frac{1}{N_{phase}}\sum_{n=1}^{N_{phase}}\frac{n-1}{N_{phase}}T_{sw} \\ &=D\cdot T_{sw}+\frac{N_{phase}-1}{2\cdot N_{phase}}\cdot T_{sw} \end{aligned} \tag{4}$$

where D is the average duty cycle, T_{sw} is the switching period and N_{phase} is the number of paralleled phases.

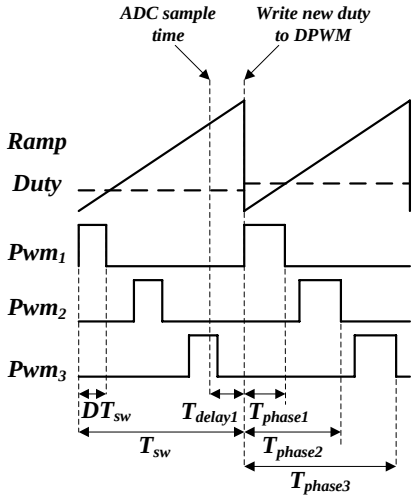

Figure 2. Phase delay in the digitally controlled system

Then taking the phase delay into account, the control-to-output transfer function can be modified as

$$G(f)=\frac{1}{e^{-sT_{delay2}}}\left(\frac{R(f)}{U(f)}-\frac{1}{C(f)\cdot e^{-sT_{delay1}}}\right). \tag{5}$$

III. Implementation Issues of Automated System Identification

A. Sinusoidal Waveform Generation

A table look-up technique is an accurate and efficient method of generating sinusoidal waveforms [13]. A table may be created in memory that holds one period of a sine wave. A sinusoidal waveform can be generated by stepping through the table, with a step size that is proportional to the desired generated signal frequency. At each sample time a new value is found from the table by adding a step increment to the previous table index into the table. If the next index points to a value beyond the table size, it is wrapped around to the beginning of the table by subtracting the table length from the calculated index value. The step increment for a given frequency f_i is defined as

$$step_i = N_{table} \frac{f_i}{F_s} \tag{6}$$

where N_{table} is the table length. Since sine and cosine values always differ by 90 degrees, the cosine values (needed for calculation in (2)) are produced by adding a quarter of the table length to the table index. The lookup table is 256 x 16 bits in the experiment; the index to the table and the step size also have 16-bit resolutions.

When a frequency is chosen that generates a non-integer number of cycles of sine wave over the measurement interval, the DFT algorithm will spread the signal energy over several frequencies, resulting in an error in the calculated magnitude. This leakage can be compensated by applying a window function to the measurement signal before multiplying by the sine and cosine reference sequences. There are several popular window functions [14] that can be applied. In the experiment, the excitation sequence is prolonged until an integer number of cycles are achieved to avoid multiplication with the window function.

B. Asynchronous Sampling

In the implementation of digital control in this experiment, the error voltage sampling frequency F_{sample} is set to be the same as the converter switching frequency F_{sw}, i.e. one error sample per switching cycle. In general, it is not necessary for the converter switching frequency F_{sw} and the perturbation injection frequency F_s to be synchronized. The asynchrony between the ADC sampling and the perturbation injection introduces an additional zero-order-hold [15] effect in the system. Figure 3 illustrates this phenomenon by resampling a f_i = 100 kHz digital sinusoidal excitation signal at F_{sw} = 350 kHz while it is injected at a rate of F_s = 800 kHz that is the maximum injection frequency the firmware can achieve in the experiment. The fundamental amplitude loss is 0.828 dB, and resampling also introduces 35.0 degrees of phase delay.

To account for the zero-order-hold effect, the DFT of the reference excitation in (5) should be adjusted as

$$R(f)^* = R(f) \cdot G_{resample}(f) \tag{7}$$

where $G_{resample}(f)$ accounts for the amplitude loss and phase lag of fundamentals for each injection frequency f_i of interest. For example, the $G_{resample}(f)$ within one half of switching frequency is shown in Figure 4, where switching frequencies F_{sw} is 350 kHz and the perturbation is injected at a rate F_s of 800 kHz. The dots indicate the loss and phase lag of 100 kHz signal in Figure 3.

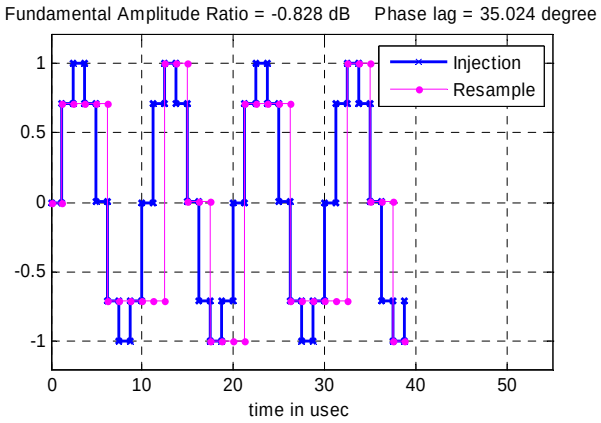

Figure 3. Asynchronous resampling

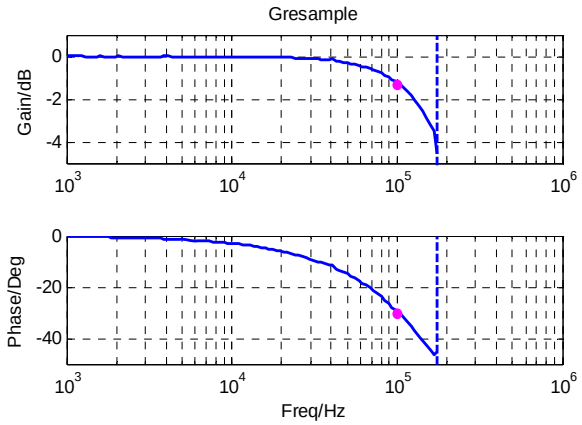

Figure 4. Characteristics of asynchronous sampling

IV. Experimental Results

Single- and multi-phase buck converters are considered to experimentally verify the system identification method. The loop gain measurements provided by a HP-3563A network analyzer are used for comparison. System parameters are listed in Table I. The digital controller is a Texas Instruments UCD9240, which provides error compensation with a two-pole/two-zero digital filter. The sine wave injection is applied to the digital reference for the output voltage, and the response is collected at the output of digital compensator. Both the digital perturbation injection and response collection are entirely performed in the UCD9240 at a rate of 800 kHz.

The test board with two single-phase and two two-phase power stages controlled by a single UCD9240 digital controller device is shown in Figure 5.

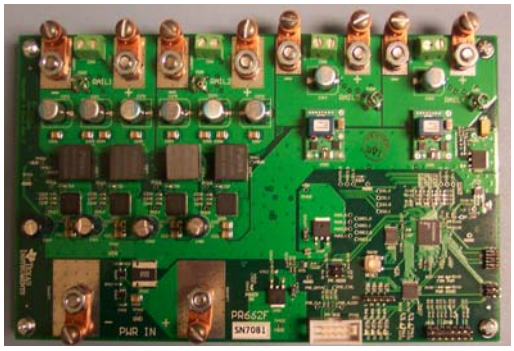

Figure 5. Overview of test board

Table I. Converter parameters

Input voltage	10 V
Output voltage	1.8 V
Load	8 A
Inductor	900 nH (DCR: 2.2 mΩ)
Capacitor, C_1	1 x 470 µF (ESR: 12 mΩ)
Capacitor, C_2	4 x 47 µF (ESR: 1.5 mΩ)
$R_{ds\text{-}on}$ of MOSFETs	3.6 mΩ
Switching Frequency	300 kHz

The loop-gain obtained from the automated identification (Auto-ID) method for a single phase converter is compared with the network analyzer results in Figure 6. The loop-gain extracted by the Auto-ID method closely matches that obtained from the network analyzer. The loop-gain from the Auto-ID method without considering the asynchronous sampling, shown in Figure 7, indicates the gain and phase discrepancies at high frequency.

The control-to-output transfer function from Auto-ID is shown in Figure 8 against predicted magnitude and phase response obtained from an average model. The characteristics of the power stage obtained from Auto-ID method matches the average model prediction, except the phase discrepancy at high frequency, which is possibly due to the parasitics of the circuits that is not included in the average model.

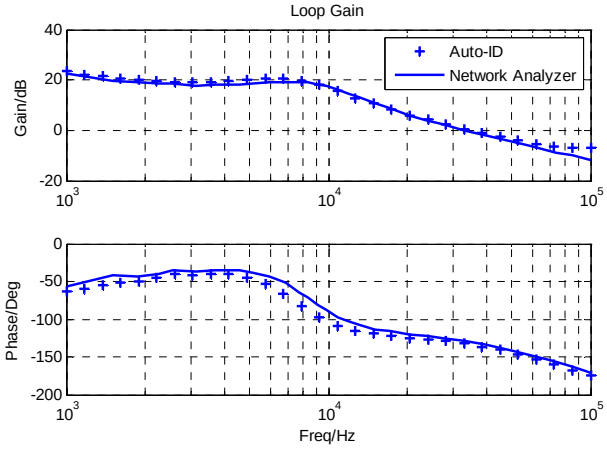

Figure 6. Loop-gain estimation of a single-phase buck converter extracted by the proposed system identification method and network analyzer

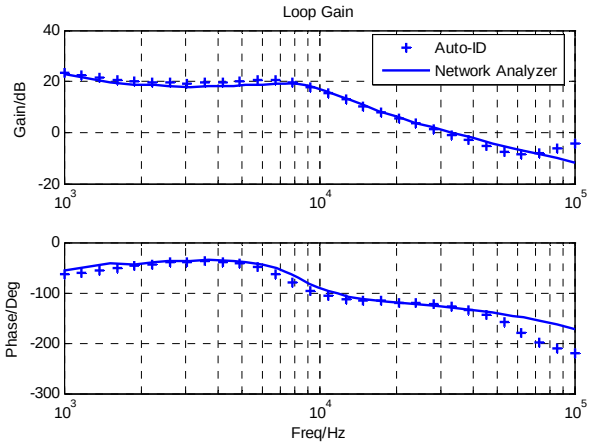

Figure 7. Loop-gain estimation of a single-phase buck converter without considering asynchronous sampling

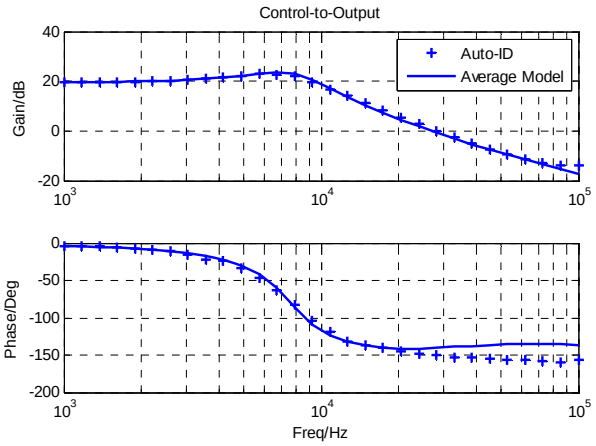

Figure 8. Control-to-output transfer function of a single-phase buck converter extracted by system identification and predicted by average model

The identification for the two-phase converter shown in Figure 9 and 10 demonstrate similar results to the single phase case. The loop-gain from the Auto-ID method is verified by the network analyzer measurement and the power stage characteristics matches the average model.

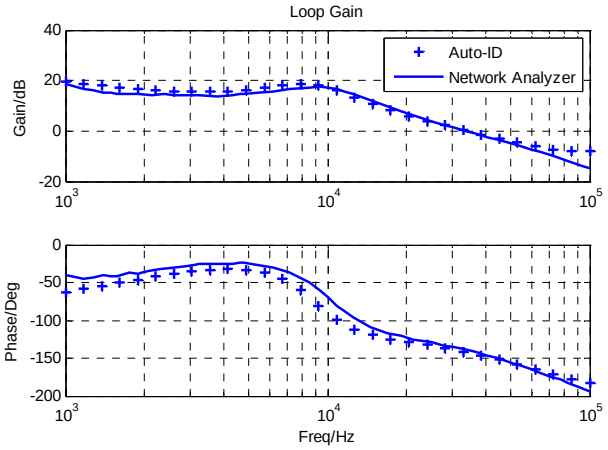

Figure 9. Loop-gain estimation of a two-phase buck converter extracted by the proposed system identification method and network analyzer

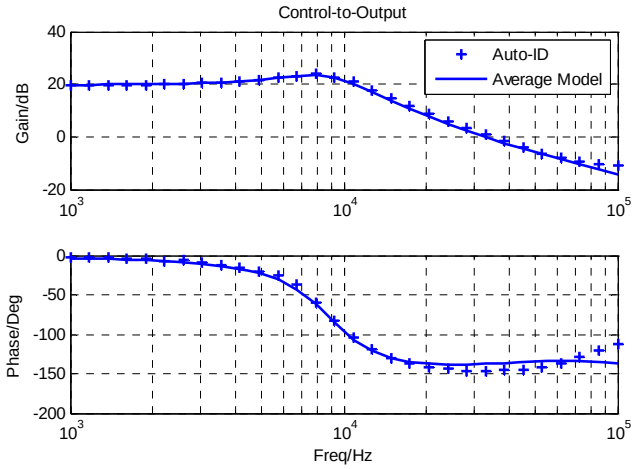

Figure 10. Control-to-output transfer function of a two-phase buck converter extracted by system identification and predicted by average model

V. CONCLUSION

An automated system identification method for digitally-controlled multi-phase DC-DC converters is set forth. Fourier analysis is utilized because of the potential for closed-loop identification and high signal-to-noise ratio. The phase loss and zero-order-hold due to digital control are considered. The identification results for single- and multi-phase DC-DC converters closely match those obtained from conventional network analyzer and average model. The proposed method can be done by a stand-alone digital controller; therefore it eliminates the requirement for expensive test equipment. The identification results can be used for controller configuration without pre-existing knowledge of the power stage parameters. This opens up a possibility of moving the determination of the loop compensation from a lab bench to a factory floor or even to an end customer's application.

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