Silicon RF Phased Array at X-, Q-, W-Band and Beyond

Kwang-Jin Koh

Virginia Tech
email: kkoh@vt.edu

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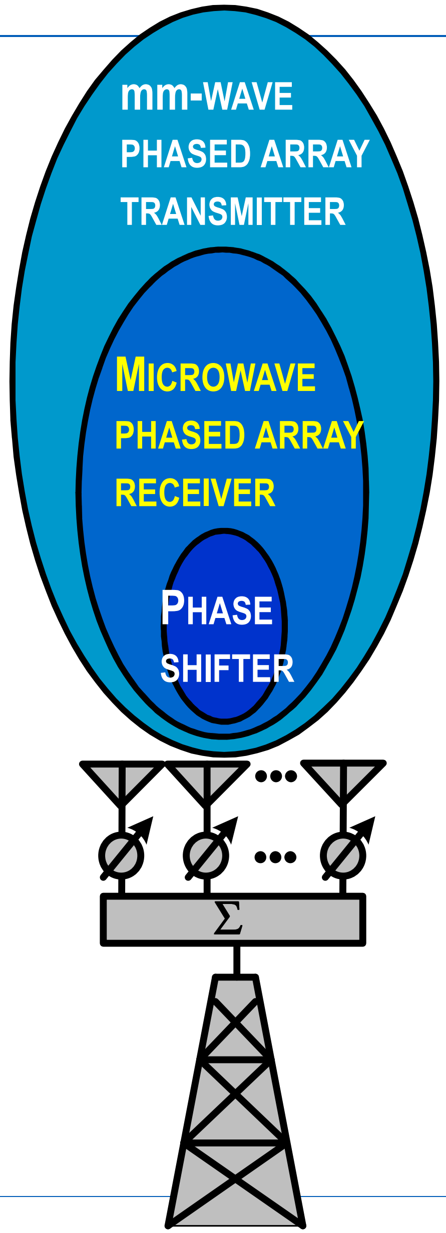
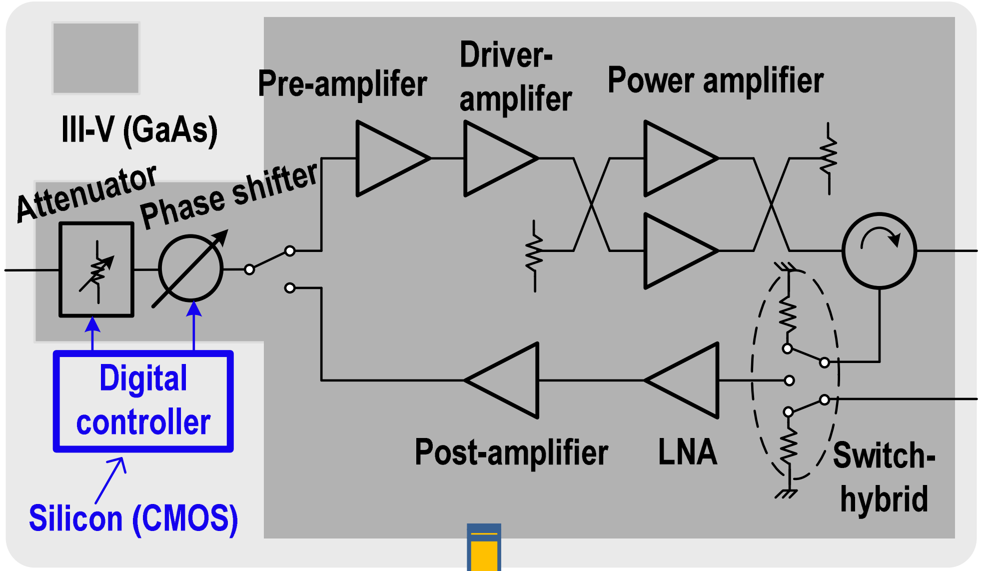
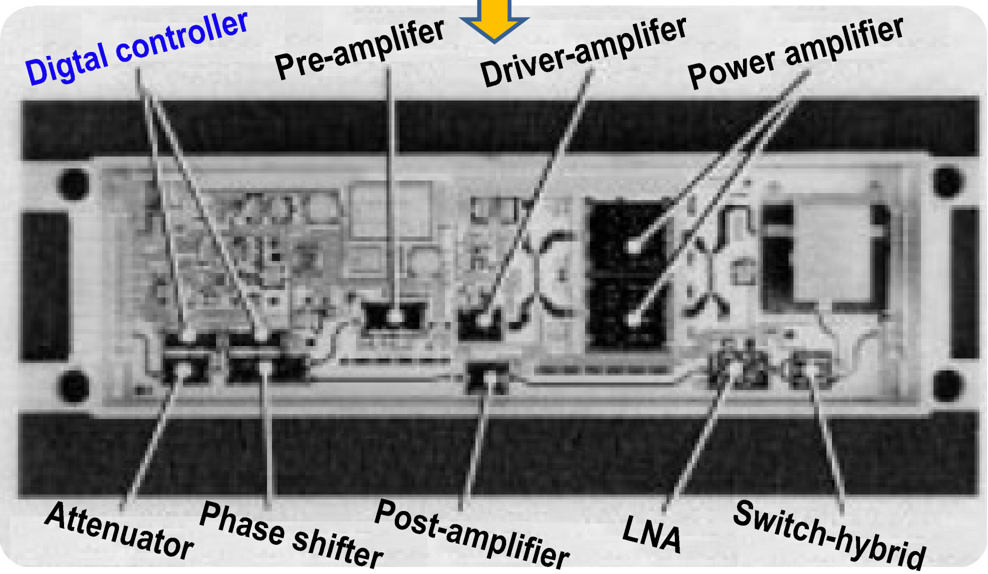
Outline

- Introduction
  - Discrete phased array: example
- Phase shifter design
  - Active phase shifter
  - Some comparisons with passive one
- Phased array designs
  - X-band receiver
  - Q-band transmitter & receiver
  - W-band & beyond
- Conclusion



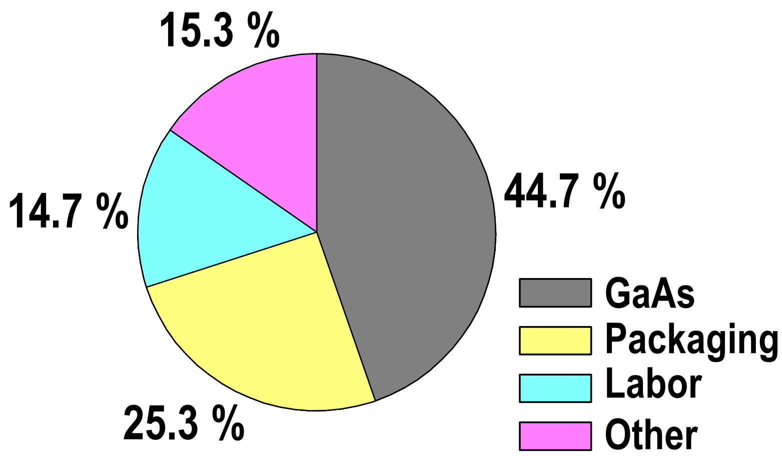
Discrete design (single element, X-band: 8-12 GHz)





TYPICAL T/R MODULE IMPLEMENTATION

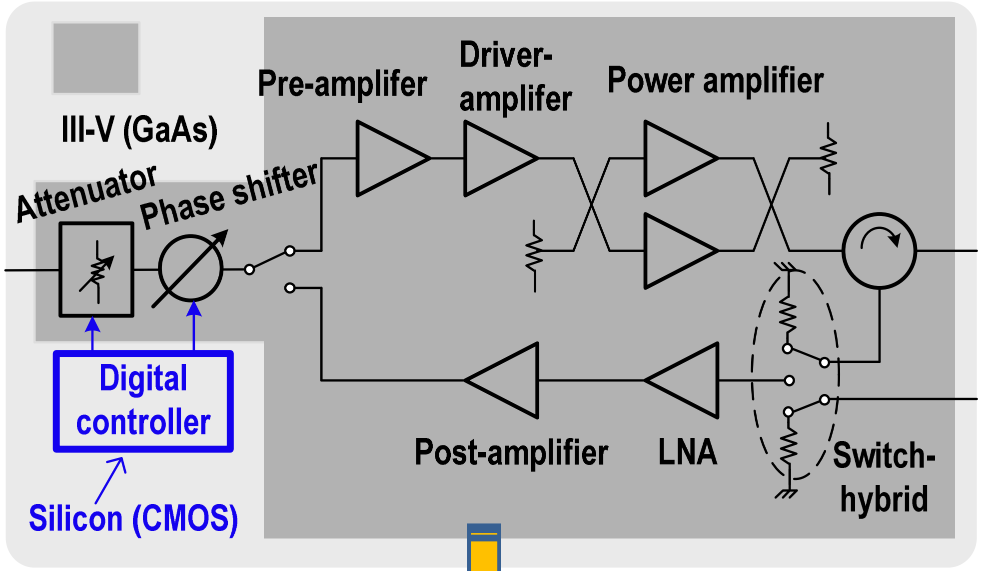
(B.A. Kopp, T-MTT, 2002)

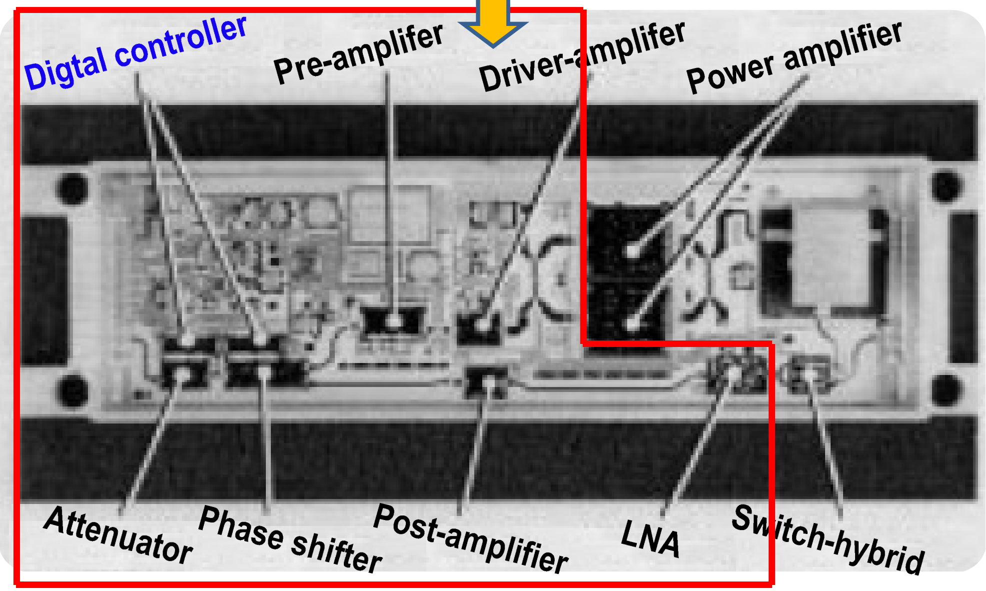


T/R module cost elements **($200-2000)**
(@ typical performance at X-band)

- III-V (GaAs) technology
- Discrete implementation: expensive & bulky
- 50-Ω interface results in high power consump.

Discrete design (single element, X-band: 8-12 GHz)

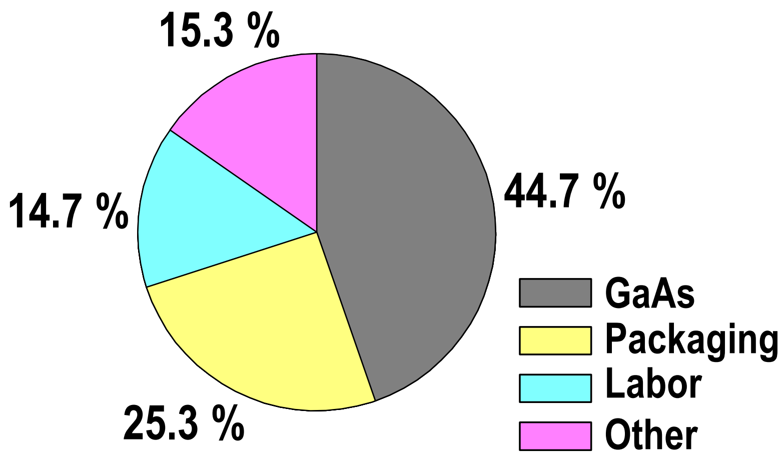




INTEGRATE THESE IN SILICON (LOW-COST PHASED ARRAY < $ 1-10)

TYPICAL T/R MODULE IMPLEMENTATION

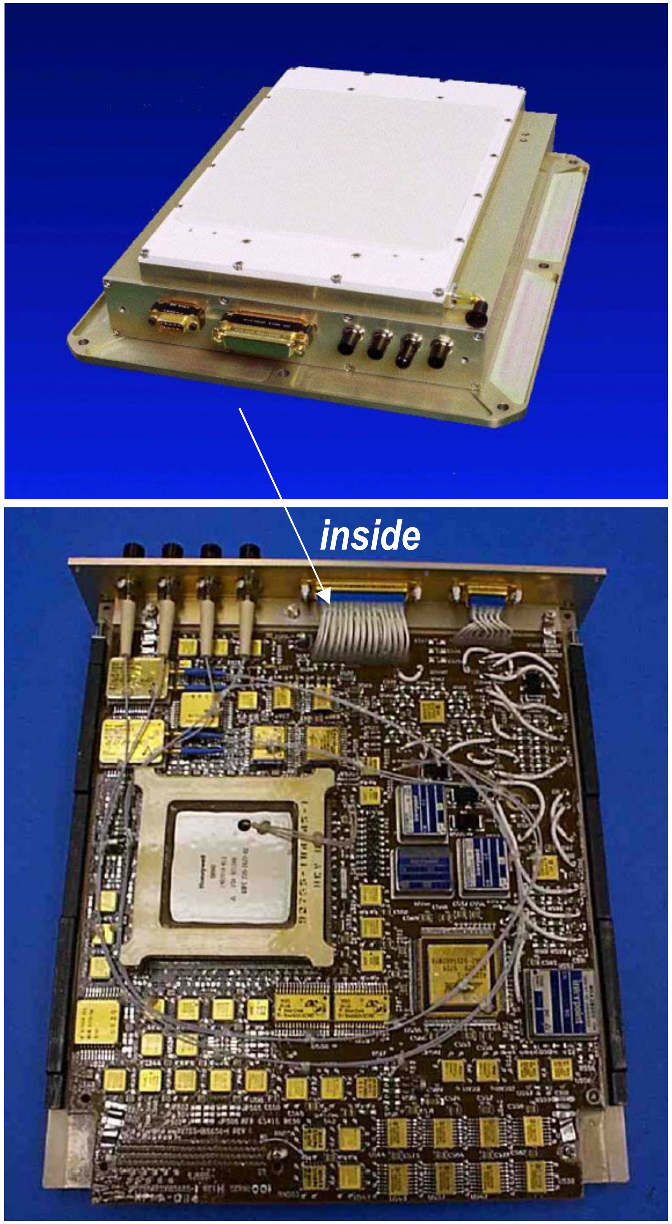
(B.A. Kopp, T-MTT, 2002)



T/R module cost elements ($200-2000)
(@ typical performance at X-band)

- Leverage recent advances in silicon tech.
- Integrate many blocks in silicon
- Low power consumption

Example: Boeing X-band array (discrete design)



64-Element X-band phased-array transmitter

(by **Boeing**, **2007 Multi-function Phased-Array Symp.**)

- Applications: satellite comm.
- Freq: 8.225 GHz (BW: 400 MHz)
- Data rate: 105 Mbps (QPSK)
- Radiation: LHCP
- EIRP: 22 dBW
- Scan angle: ±60°
- Phase update rate: 2°/second

- Weight: 5 kg
- Envelop size: 25 x 36 x 15 cm^3
- Power consumption: 45 W

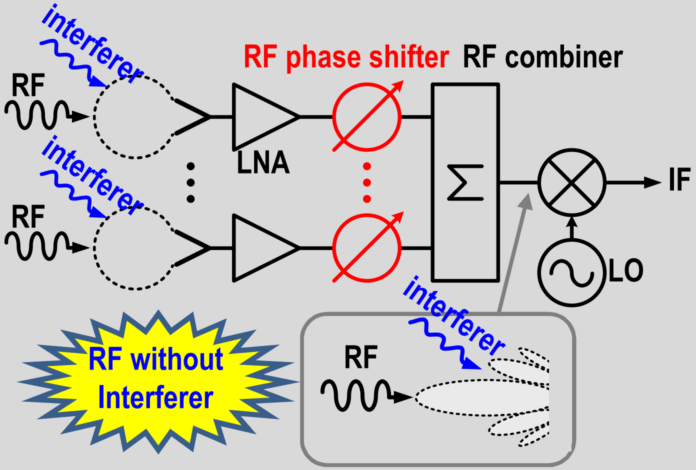
Watch for these numbers ! We want to minimize them.

- 4-bit RF phase shifter
- Power gain (ave): 22 dB per channel
- OP1dB: 18 dBm per channel
- PAE: 22 % (@P1dB)
- Temp: 0-40°C

Could be possible in silicon (SiGe BiCMOS or CMOS) !

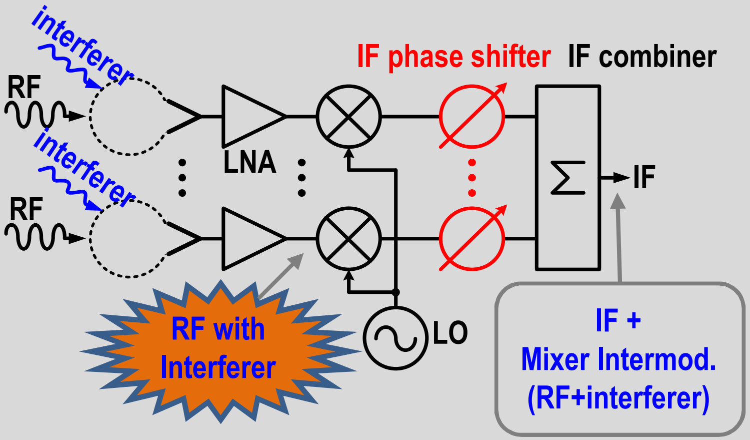
Integrated phased-array architectures

RF-SCANNED PHASED ARRAY



- Need 1 mixer (simple)
- Mixer "sees" high directivity pattern
- Favorable to scalability (> ~100's # of array)
  - RF combiner can be simple, e.g. adder amp
- Widely used (since 1950)

IF (LO)-SCANNED PHASED ARRAY



*LO-phase shifting is equivalent to IF-phase shifting

- Need # N mixers (complex)
- Mixer "sees" low directivity pattern
- Not favorable to scalability (< ~10's # of array)
  - Complex LO distributions, coupling …
- Limited applications

- RF-scanned array can achieve high integration level
- RF phase shifting architecture meets backward compatibility with existing systems
- **RF-scanning array is favored by industry: LM, Boeing, Teledyne, IBM, MTK, Intel, …**

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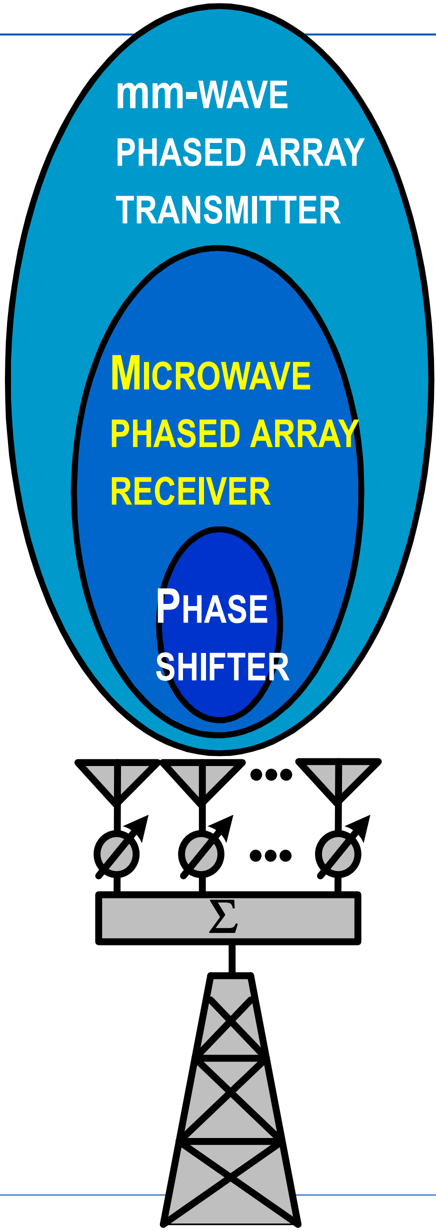
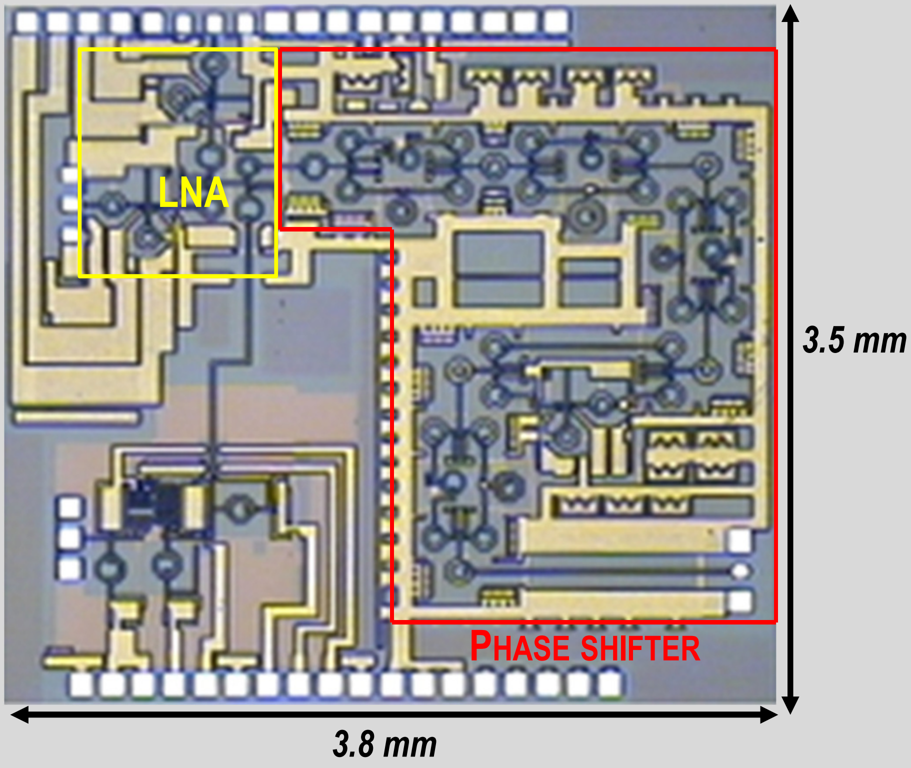


Typical passive phase shifter (example)

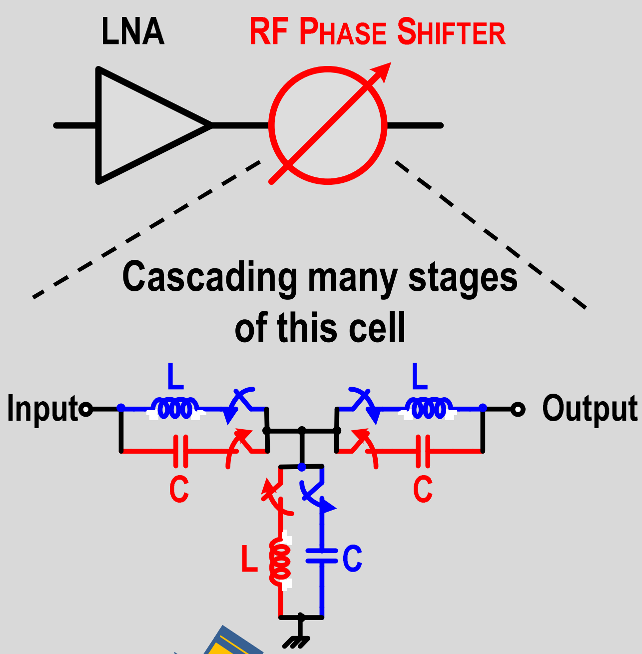


Ref: Comeau etal (Georgia Tech), "A SiGe Receiver for X-Band T/R Radar Modules", IEEE JSSC, Sept. 2008

- Freq: 8-10.7 GHz (Δ=2.7 GHz, < 25% BW)
- Phase resolution: 5-bit (11.25°)
- RMS phase error < 9°
- ~ 36 inductors
- Loss ~ 20 dB
- Area > 8 mm²

→ Issues: area & loss

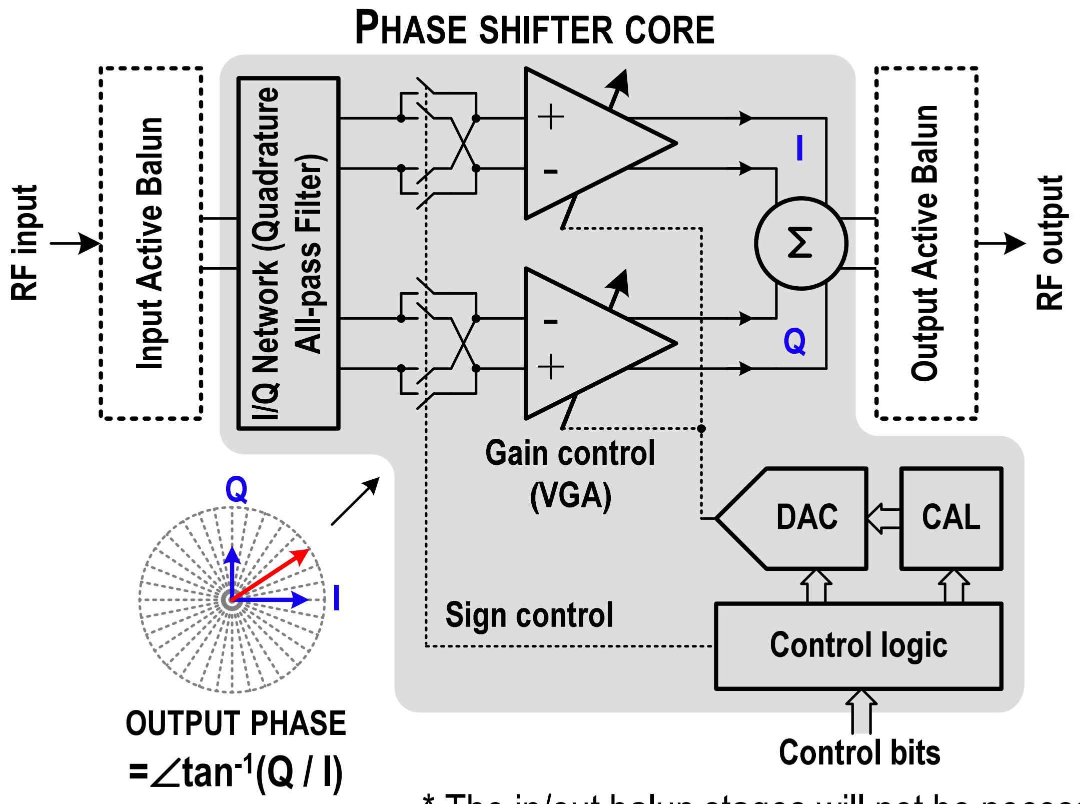
LOW-PASS / HIGH-PASS APPROACH



- Blue path: low-pass
→ Phase lagging
- Red path: high-pass
→ Phase leading

Utilize phase difference

Active phase shifter architecture: vector modulator



Operation

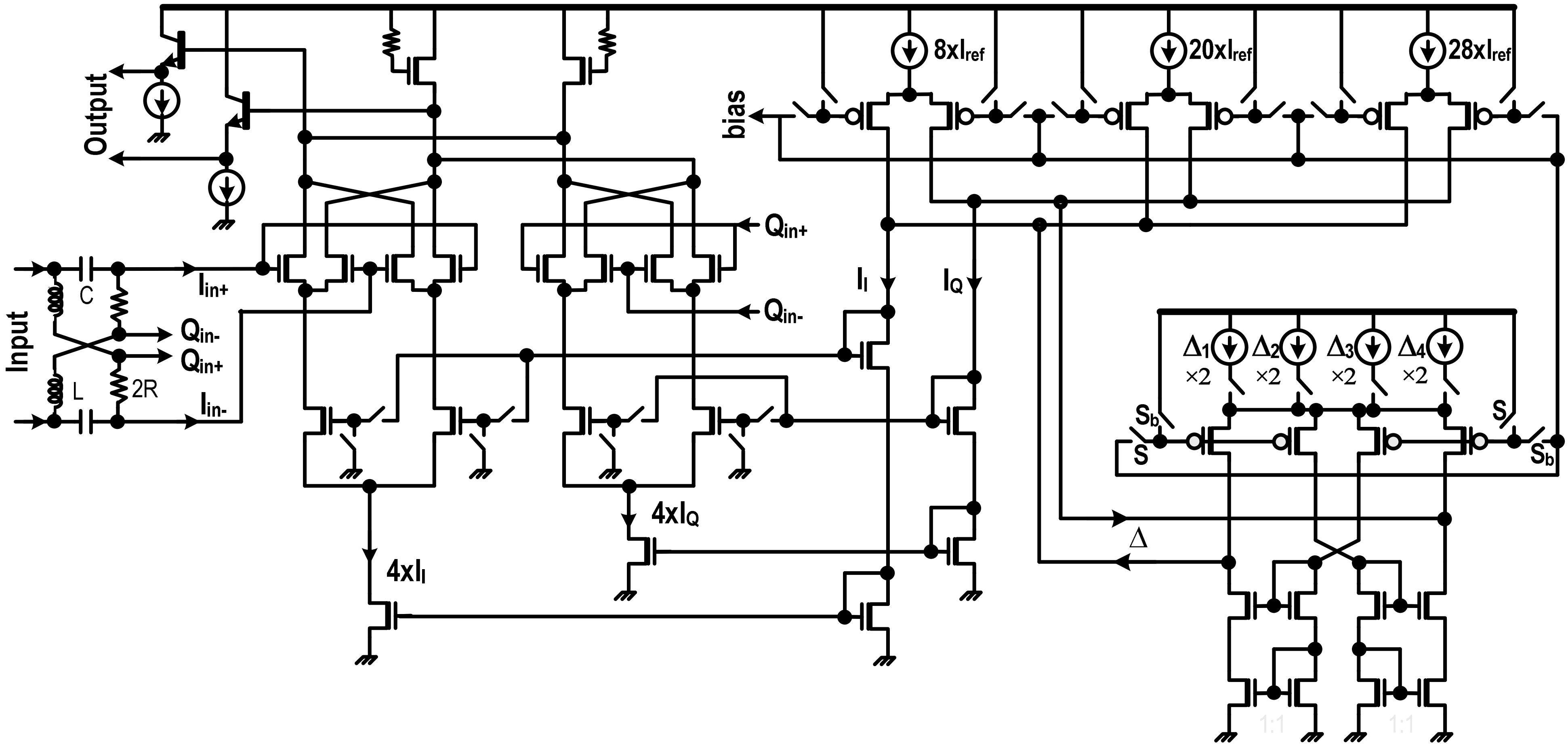
- Balun provides differential signal
- I/Q network splits signal into I & Q vector signals
- VGA controls gain for I & Q path
- I/Q signals are added in V-domain (phase interpolation)
- DAC provides 4-bit phase control
- CAL calibrates DAC to get 5-bit phase resolution

* The in/out balun stages will not be necessary for fully integrated differential systems

Mostly active circuits ⇨ Small chip area & Gain

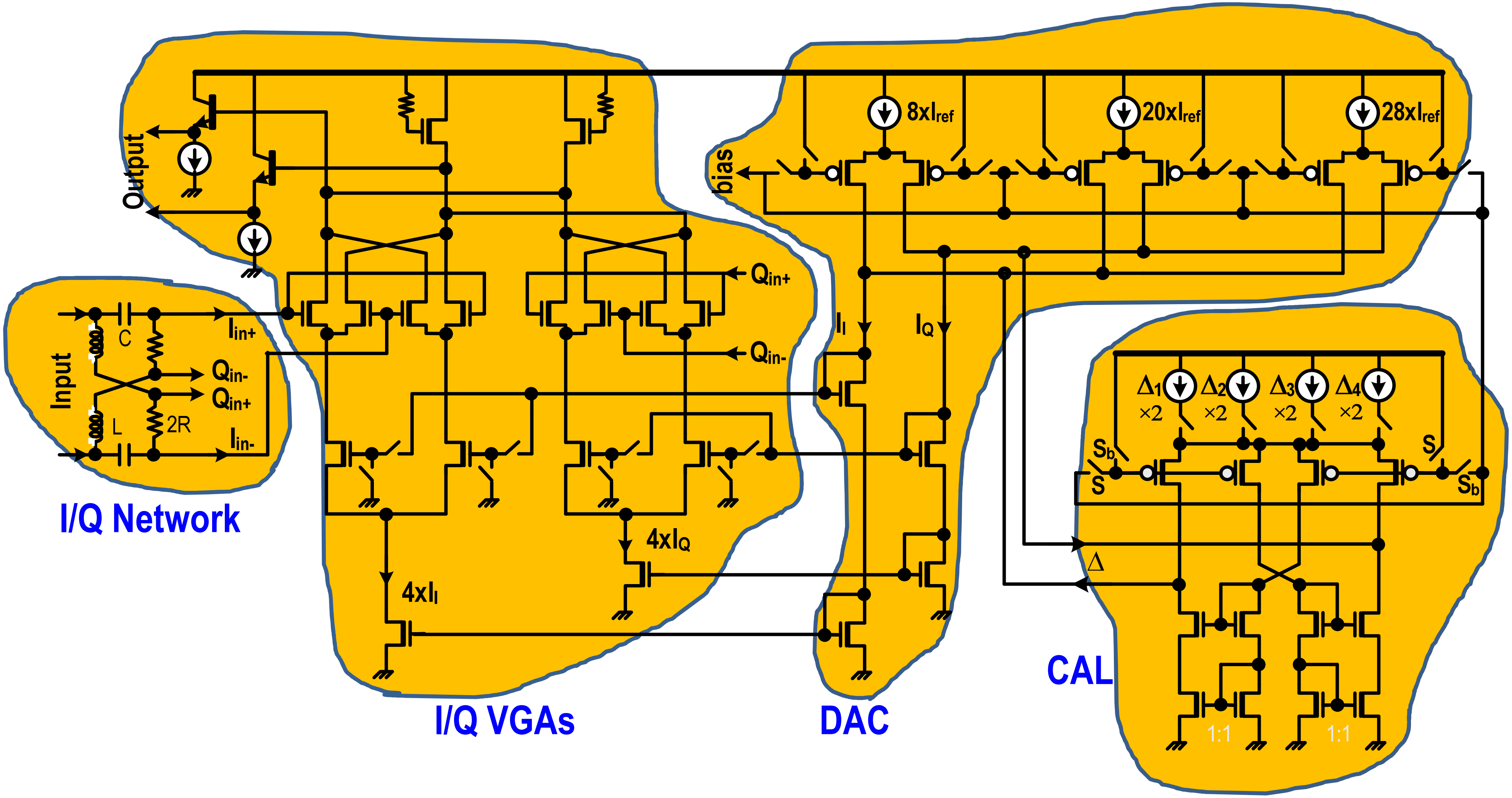
DAC control ⇨ Fine accurate phase control & calibration

Active phase shifter - schematic



Ref: K.-J. Koh etal, "0.13-µm CMOS phase shifters for X-, Ku-, and K-Band Phased Arrays", IEEE JSSC, Nov. 2007

Active phase shifter - schematic



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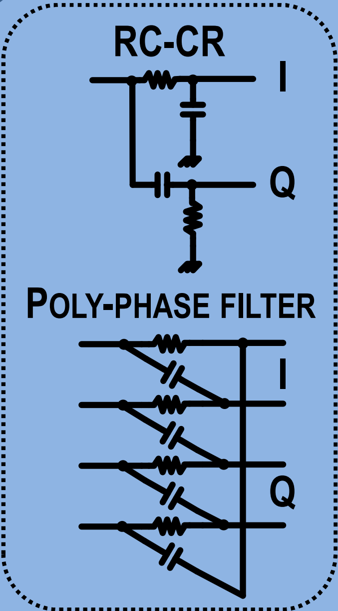
Active phase shifter - I/Q network



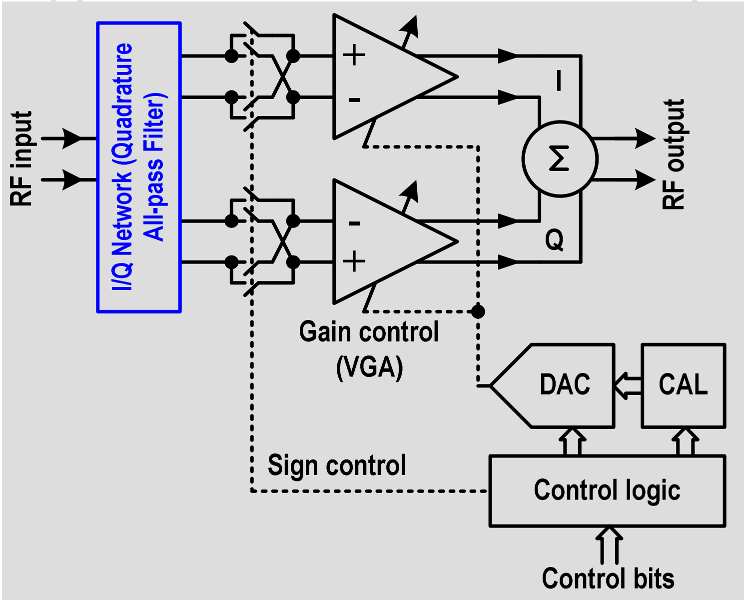
CONVENTIONAL DESIGNS

RC-CR, POLY-PHASE FILTER

➡ **Mostly suffer from loss**

QUESTION:

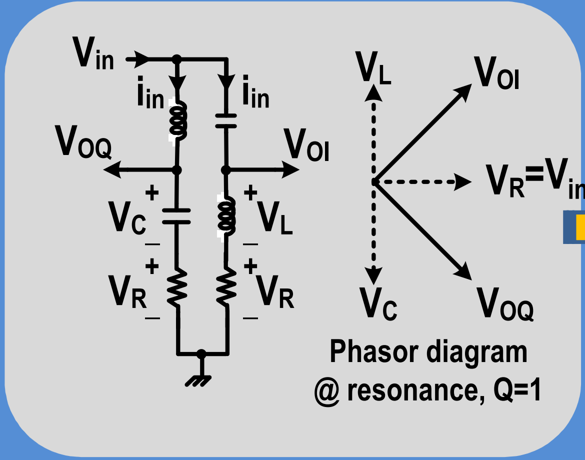
How can we make a lossless I/Q network ?



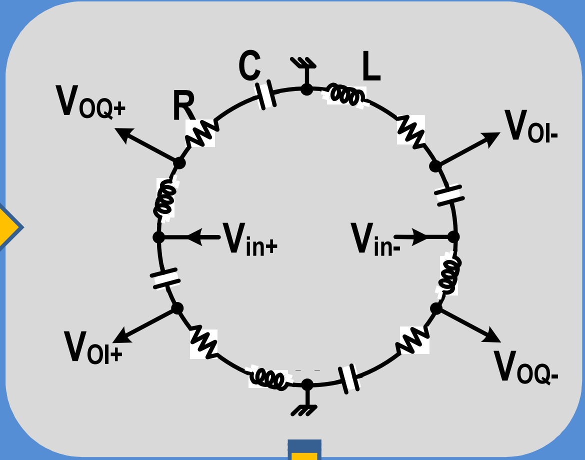
Proposed lossless I/Q network

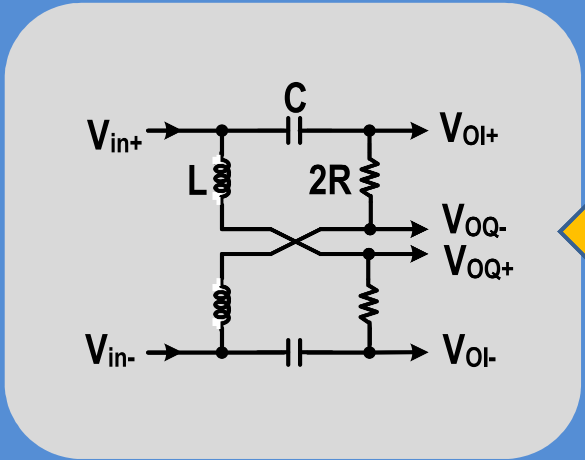
Passive signal interpolation for quadrature vector synthesis !

1. Single-ended quadrature generation

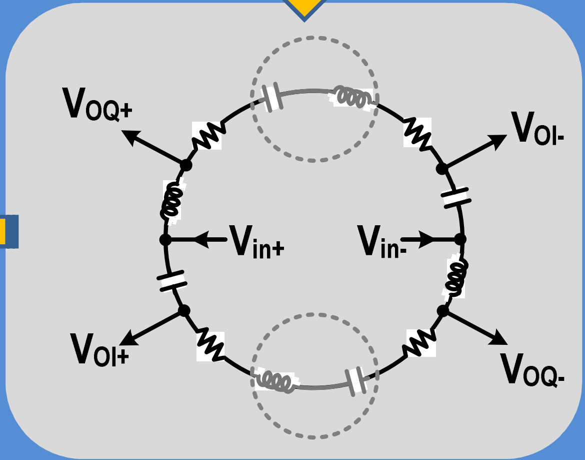


2. Differential configuration





4. Differential **Q**uadrature **A**ll-pass **F**ilter (QAF)



3. Elimination by series resonance

NOTE

- Step-1: 3-dB gain @ resonance
- Step-3: bandwidth extension (by removing L-C energy storage pair, de-Q)
- All-pass filter with 3dB NF

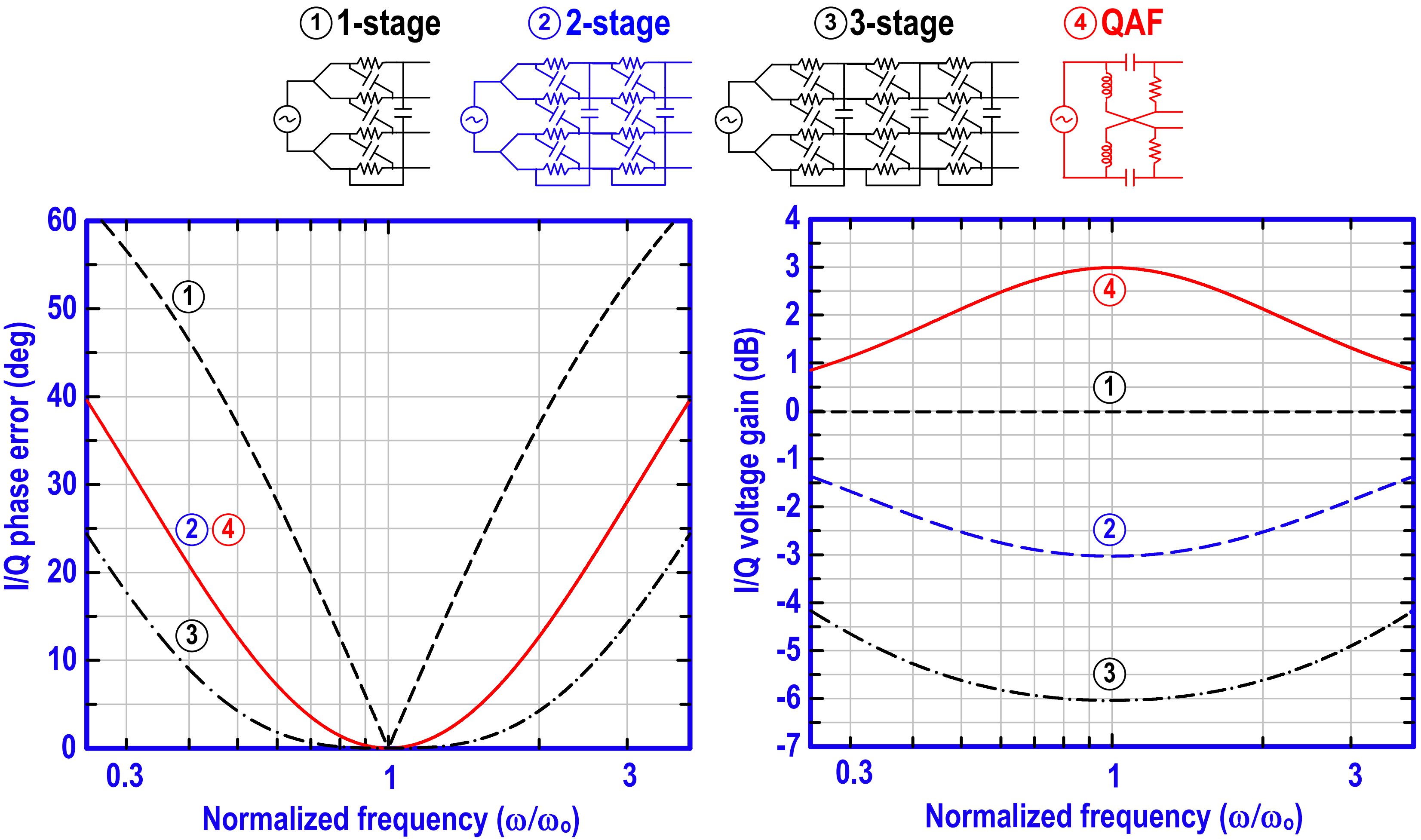
TRANSFER FUNCTION

$$\begin{pmatrix} V_{OI\pm} \\ V_{OQ\pm} \end{pmatrix} = V_{in\pm} \times \begin{pmatrix} \underbrace{\dfrac{s^2 + \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}s + \omega_o^2}}_{\text{I-path}} \\ \overbrace{\dfrac{s^2 - \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}s + \omega_o^2}}^{\text{Q-path}} \end{pmatrix}$$

$$\text{where, } Q = \frac{\omega_o L}{R}, \ \omega_o = \frac{1}{\sqrt{LC}}$$

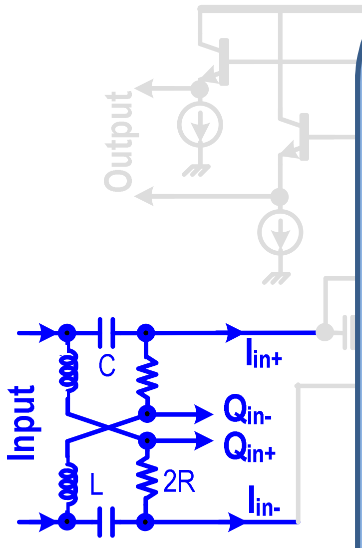
Ref: K.-J. Koh etal, "0.13-µm CMOS phase shifters for X-, Ku-, and K-Band Phased Arrays", IEEE JSSC, Nov. 2007

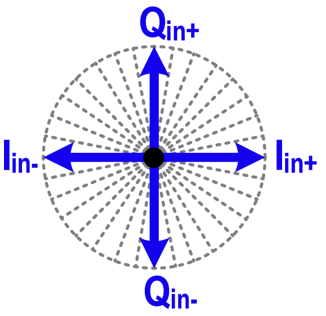
Proposed lossless I/Q network - comparison



- Exactly the same I/Q phase performance as the 2-stage polyphase filter.
- But, 6 dB larger voltage gain than the 2-stage polyphase filter.

Active phase shifter - I/Q network (lossless)

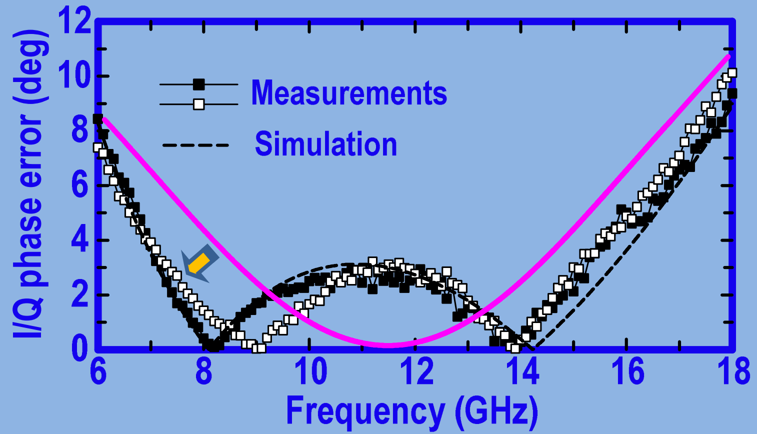




For X- & Ku-Band (6-18 GHz)

- 2R=50 Ω
  L=324 pH
  C=543 fF ➡ f_o=12 GHz

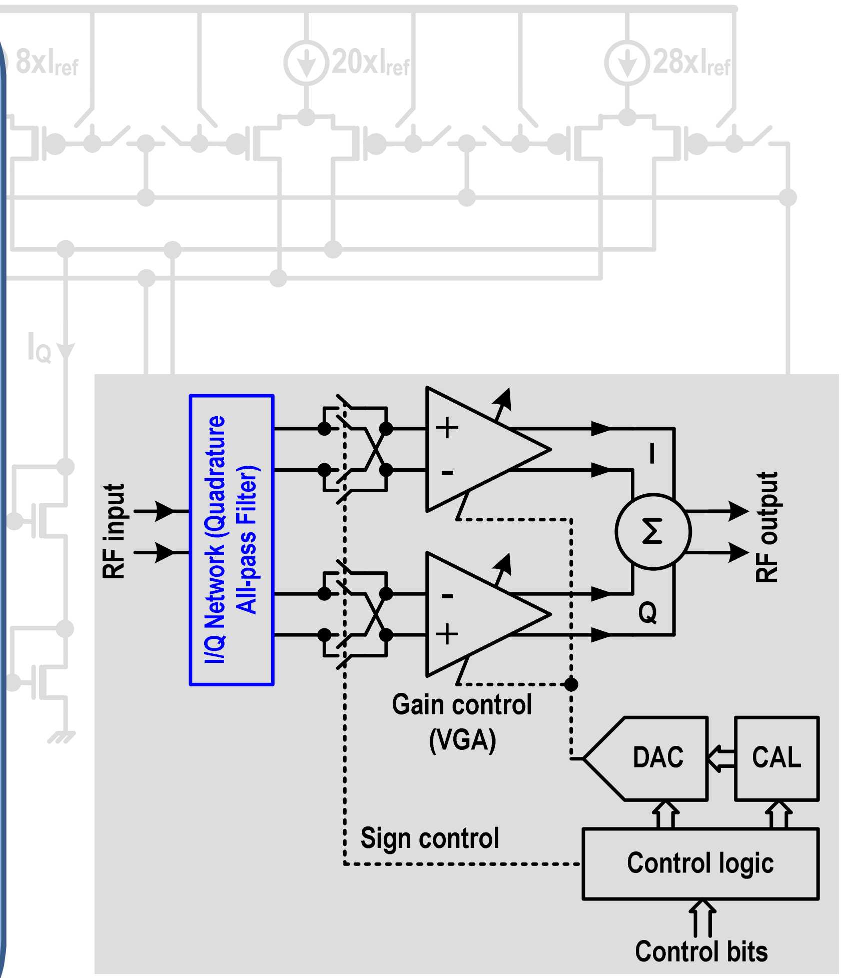
- Optimization of R, L & C
  ➡ Allow acceptable error around f_o to increase bandwidth.



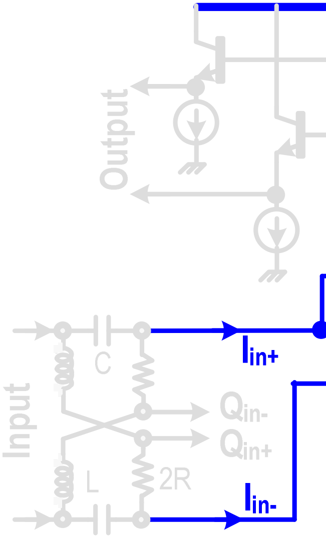
Under 70 fF loading capacitance,

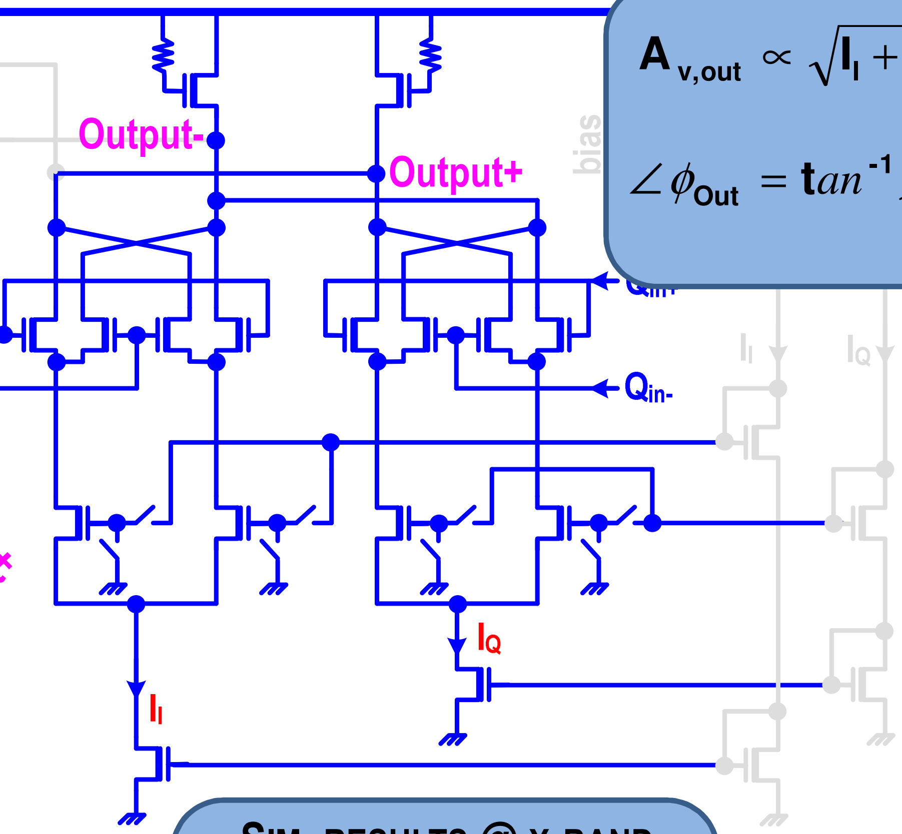
I/Q phase error < 3° @7-15 GHz

I/Q amplitude mismatch < 1.8 dB @7-15 GHz



Active phase shifter - I/Q VGAs (vector modulator)

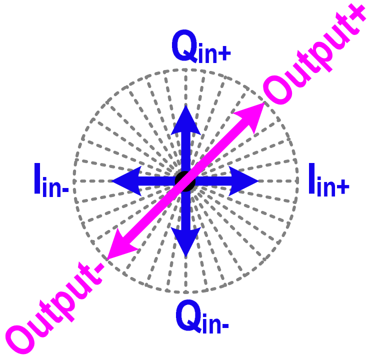


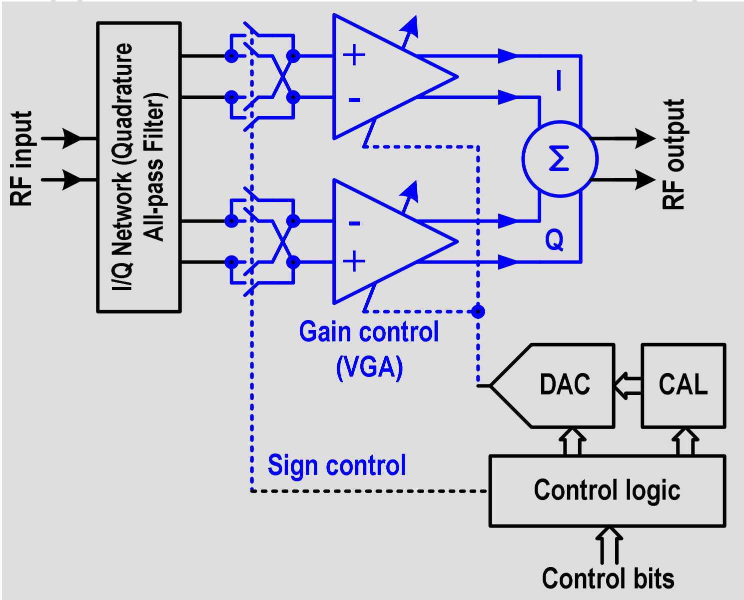


$$A_{v,out} \propto \sqrt{I_I + I_Q}$$

$$\angle \phi_{Out} = \tan^{-1}\sqrt{\frac{I_Q}{I_I}}$$

- 2 Gilbert-cells ➡ I/Q VGA
- Active inductor ➡ save area
- Keep I_Q+I_I=constant
  ➡ constant gain versus phase change



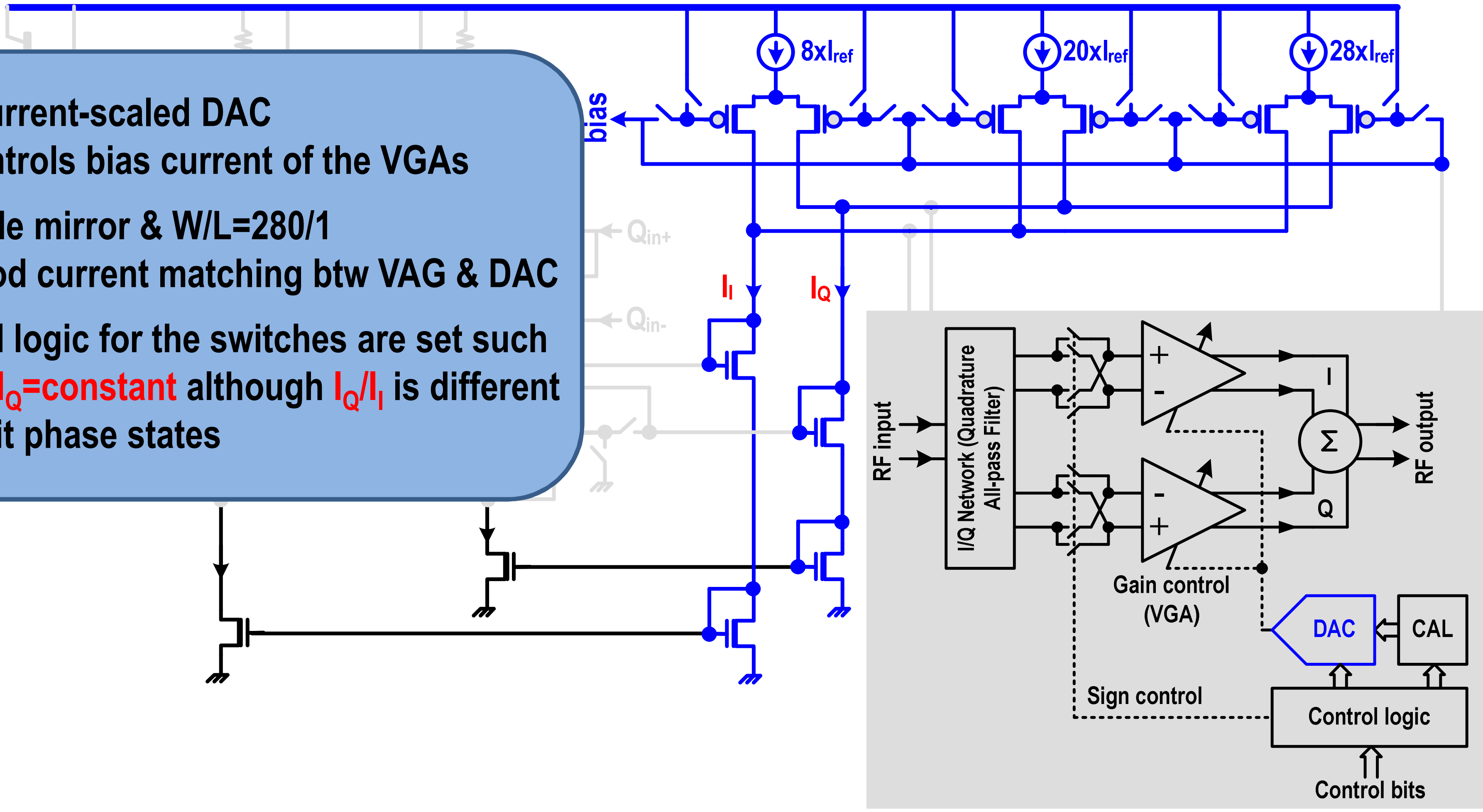


SIM. RESULTS @ X-BAND

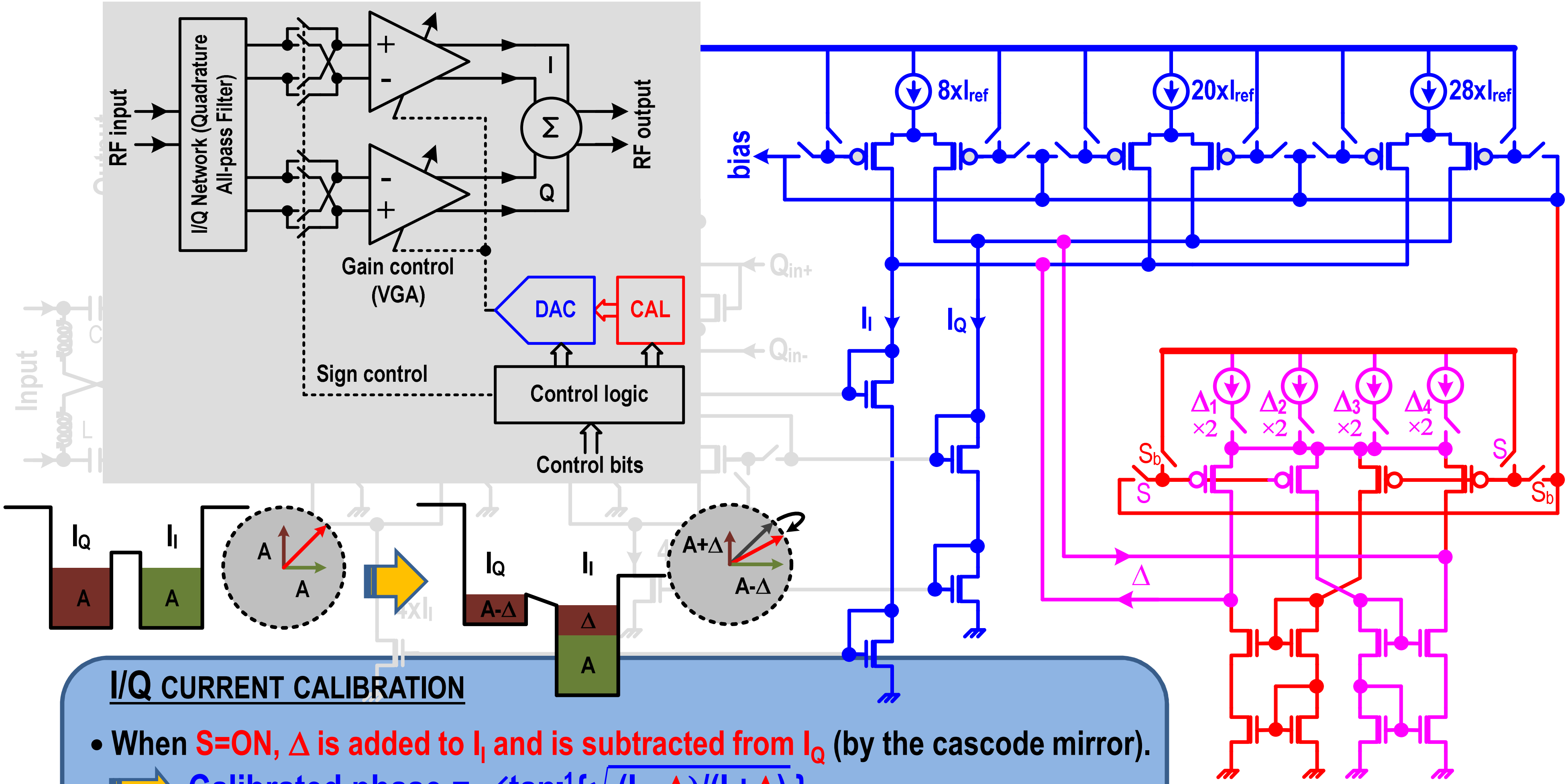
- 0.18-µm CMOS
- Gain = 0 dB @12 GHz
- IIP3 = 15 dBm @12 GHz
- I_I+I_Q=2.5 mA, Vdd=3.3 V

Active phase shifter - DAC

- 3-bit current-scaled DAC
  ➡ controls bias current of the VGAs
- Cascode mirror & W/L=280/1
  ➡ good current matching btw VAG & DAC
- Control logic for the switches are set such that I_I+I_Q=constant although I_Q/I_I is different for 4-bit phase states



Active phase shifter - CAL



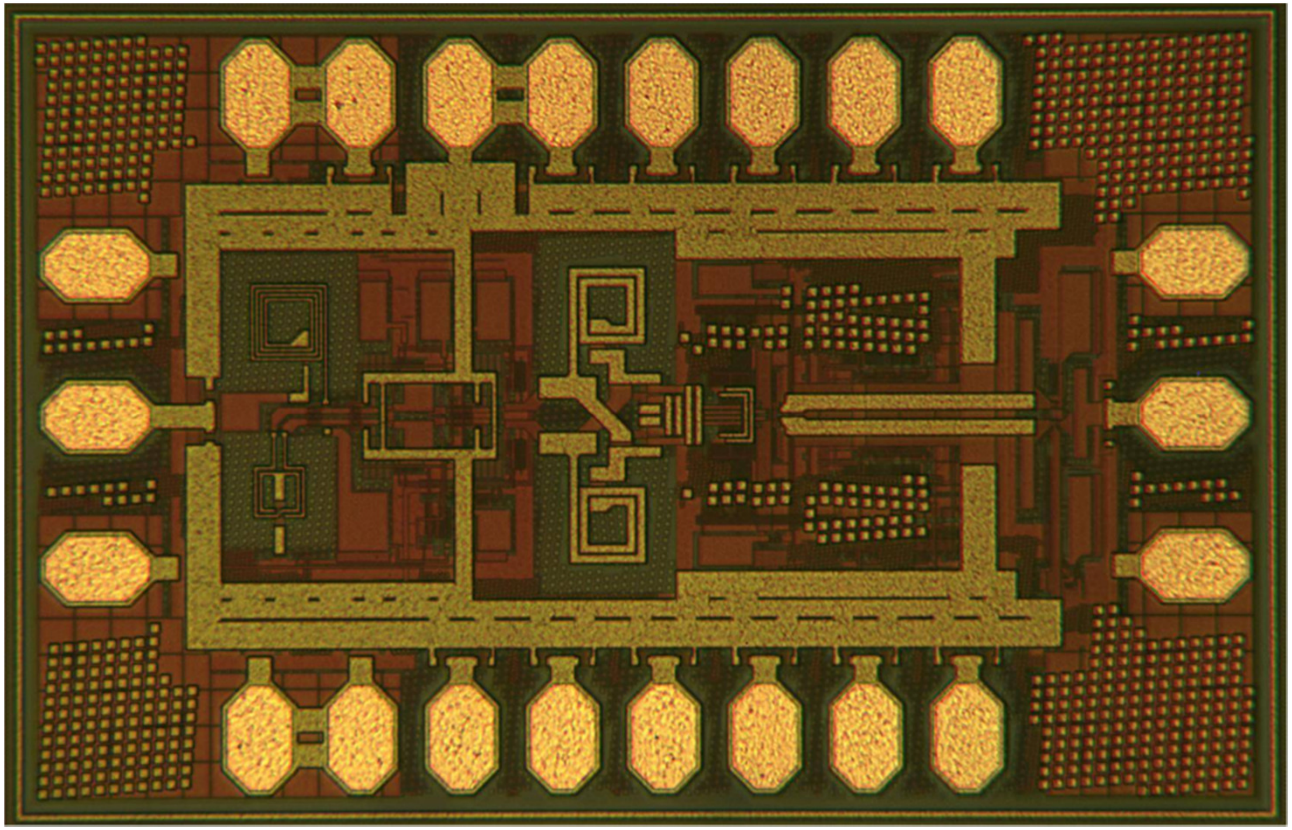
I/Q CURRENT CALIBRATION

- When S=ON, Δ is added to I_I and is subtracted from I_Q (by the cascode mirror).

  ⇨ Calibrated phase = $\angle\tan^{-1}\{\sqrt{(I_Q-\Delta)/(I_I+\Delta)}\}$

- When S=OFF, the direction of Δ is reversed.
- Still, I_I+I_Q=constant ⇨ gain is same after calibration.

Active phase shifter – chip photo



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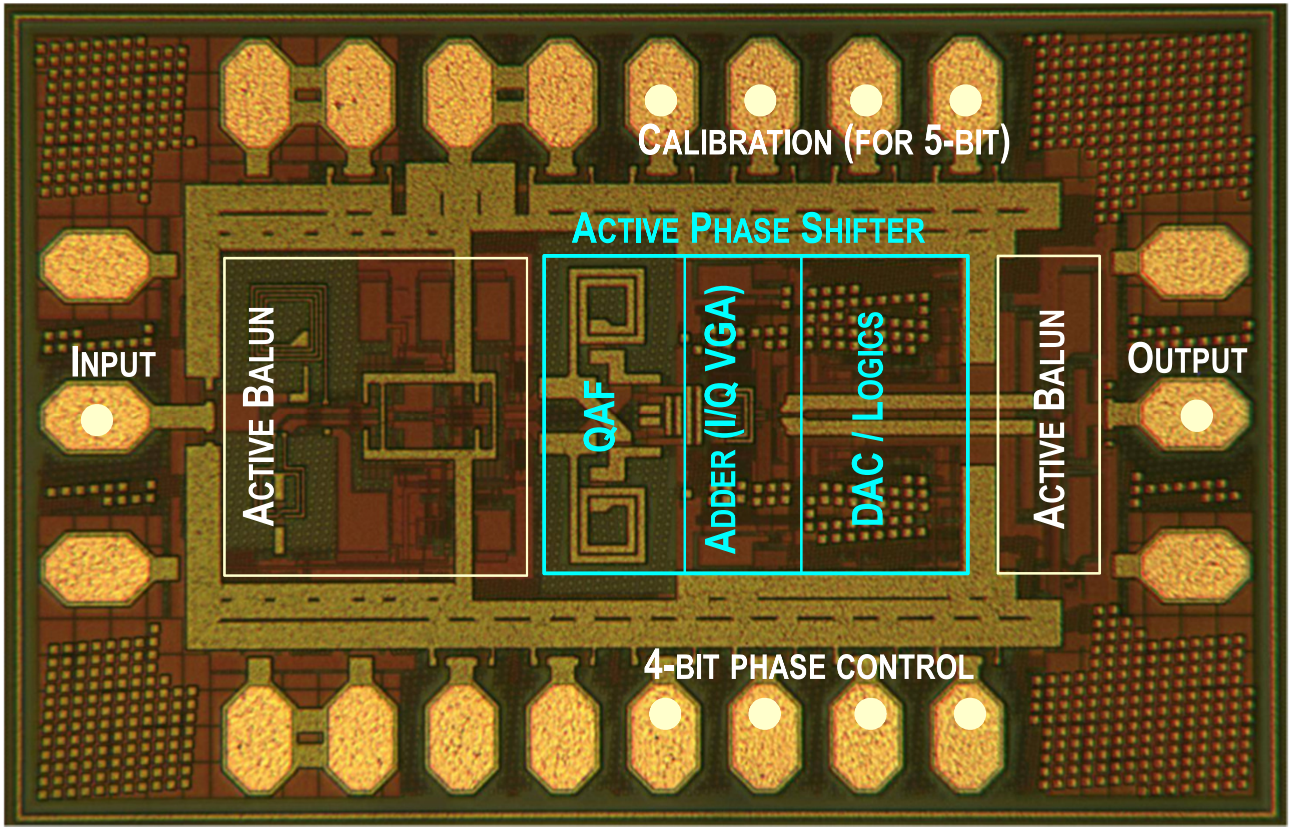
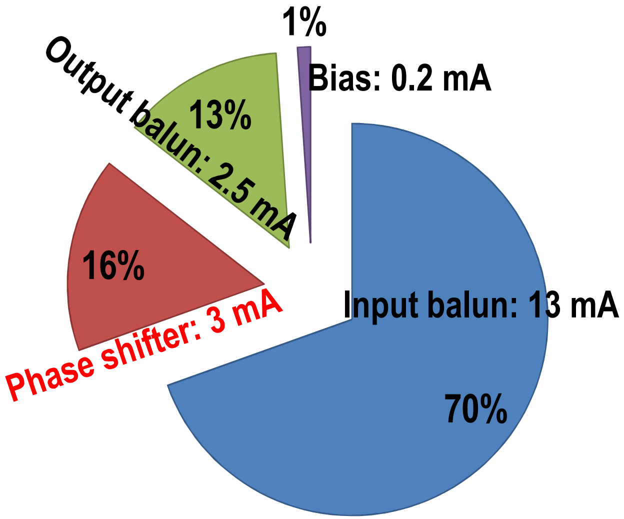


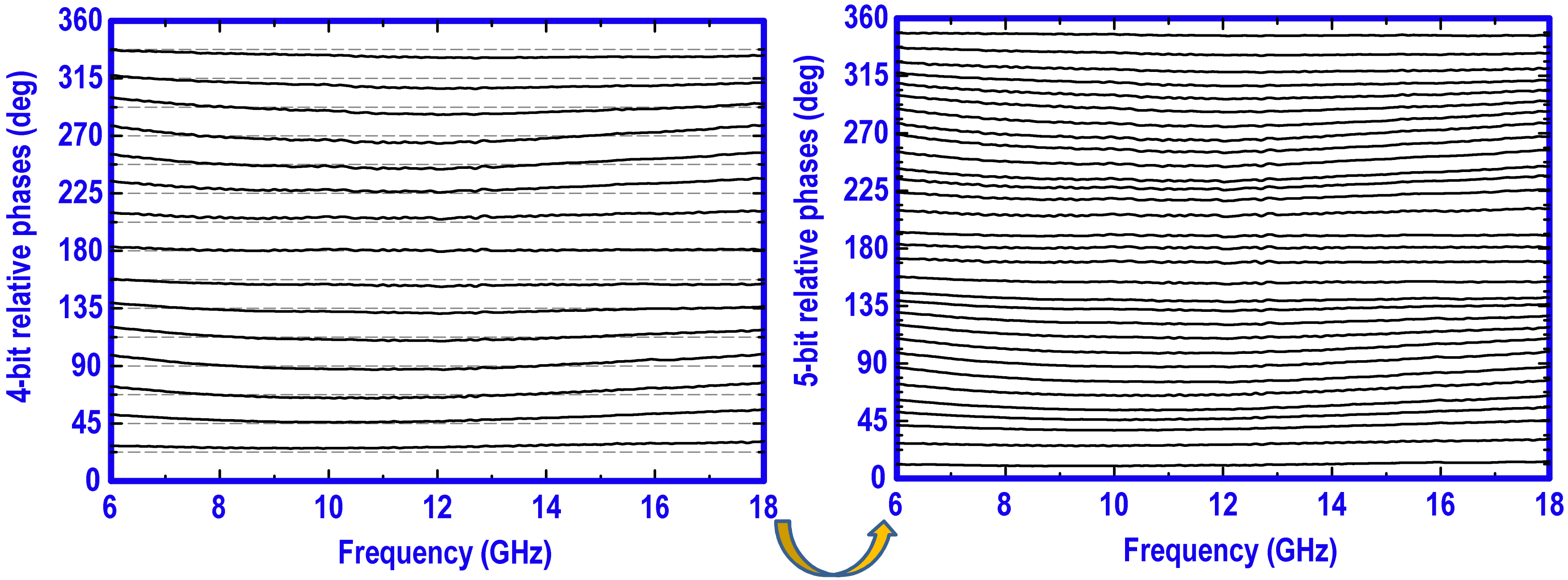
- 0.18-µm SiGe BiCMOS process
(Phase shifter: 0.18-µm CMOS)
- Chip size: 1.2 x 0.7 mm^2
(Phase shifter: 0.4 x 0.3 mm^2)
- Total current: 18.7 mA (V_{DD}=3.3 V)



- All pads are ESD protected
(HBM rating: 3kV, 2A)

- Supported by "DARPA SMART project" (2006-2008)
- Presented at the DARPA meeting & MTT-s 2010
- Lockheed Martin bought the designs (schematic & layout), 2009

Active phase shifter – 4/5-bit relative phases



After DAC calibration

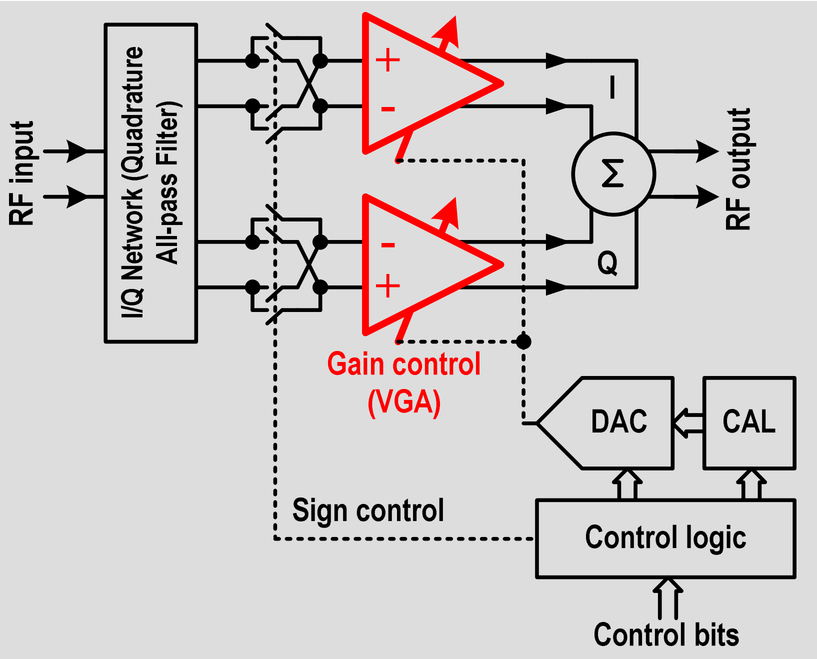
(Relative phases referenced to 0°-bit phase, RMS phase error < 5.6° @6-18 GHz)

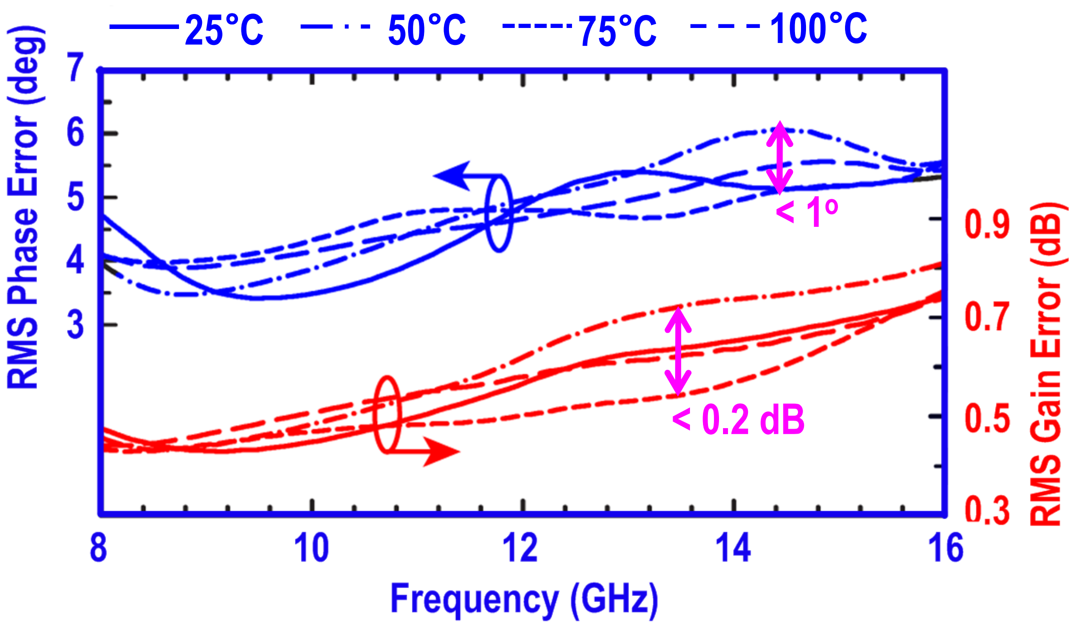
NOTE

- Phase interpolation is an independent process of frequency
- Operational BW is limited by the I/Q network, i.e. the accuracy of I/Q network
- Phase can be easily calibrated using a high resolution DAC (not easy in passive design)

First realization of integrated 5-bit active phase shifter in silicon achieving 6-18 GHz coverage (3:1 BW)

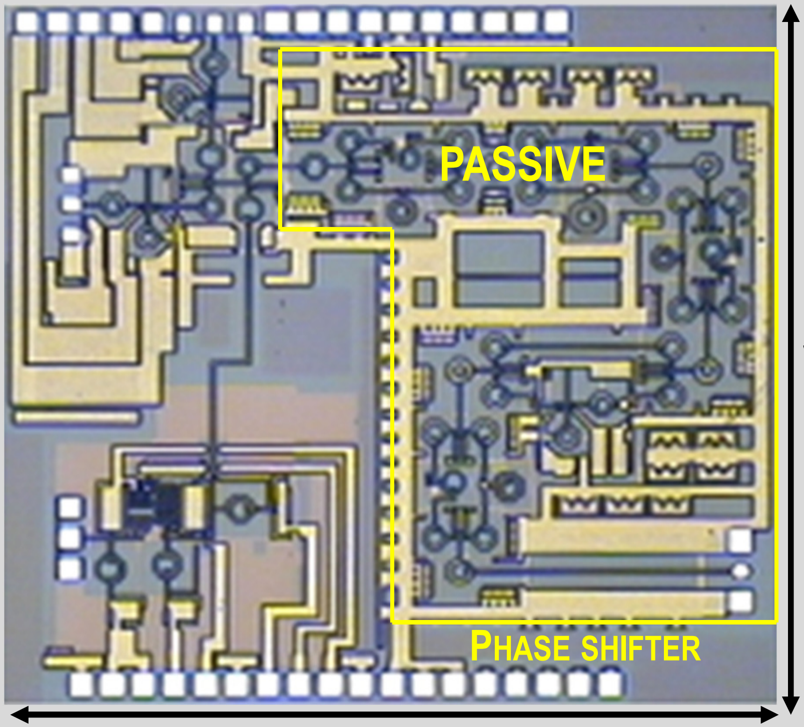
Active phase shifter – temperature measurements





- I & Q paths are biased with a reference PTAT circuit
- Output phase depends on I:Q gain ratio (not absolute gain)
- I & Q amplifiers track each other vs. PVT, resulting in low sensitivity to PVT
- RMS phase error < 6° @ 25°-100° C

Comparison: passive vs. active phase shifter



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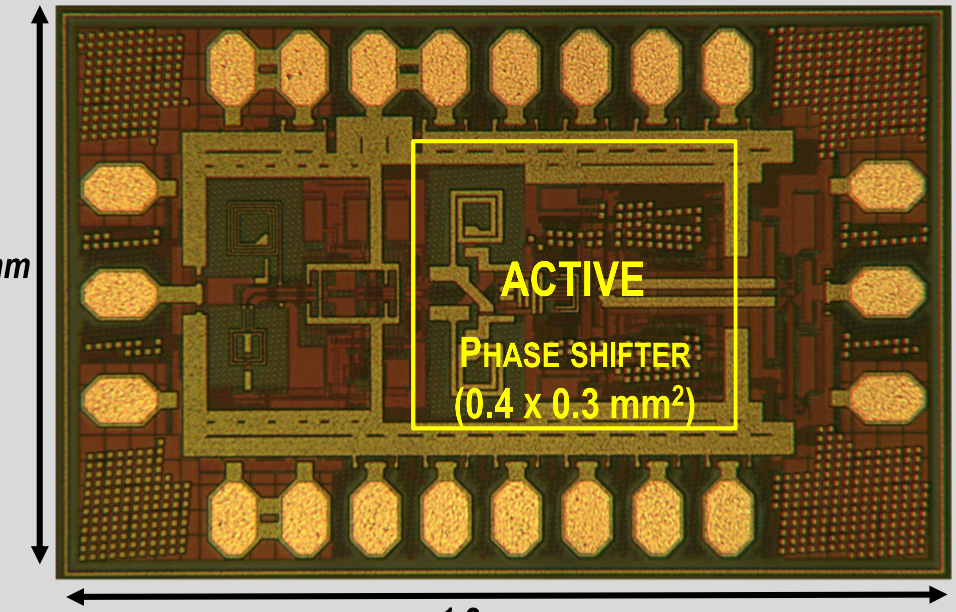
- Freq: 8-10.7 GHz (Δ=2.7 GHz, < 25% BW)
- Phase resolution: 5-bit (11.25°)
- RMS phase error < 9°
- ~ 36 inductors
- Loss ~ 20 dB
- Area > 8 mm² (> 65x active design)

Compare



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Ref: K.-J. Koh etal, "A 6-18 GHz 5-bit active phase shifter", IEEE MTT-S, May 2010

- Freq: 6-18 GHz (Δ=12 GHz, 3:1 BW)
- Phase resolution: 5-bit (11.25°)
- RMS phase error: < 5.6°
- 2 inductors
- Loss ~ 0 dB
- Area: 0.12 mm² (smallest one published)

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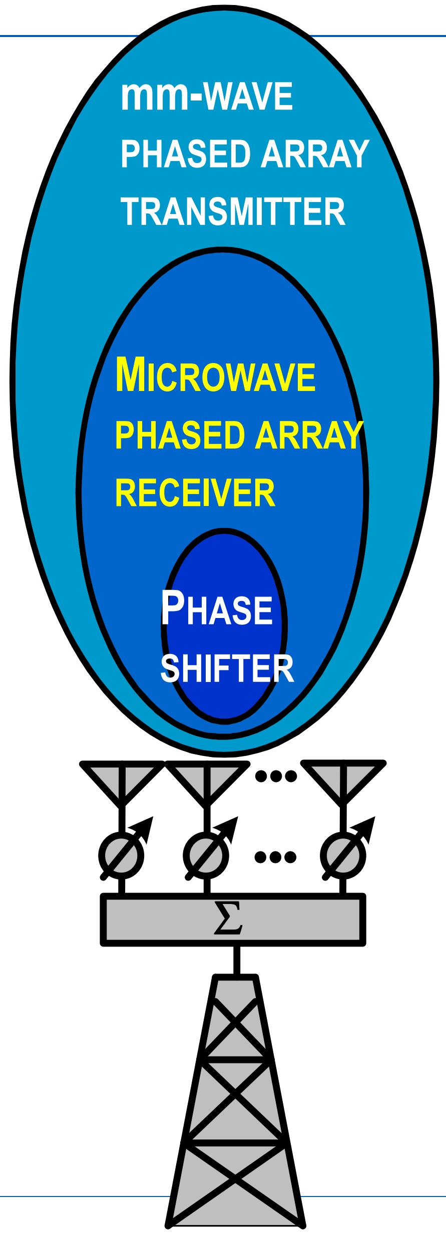
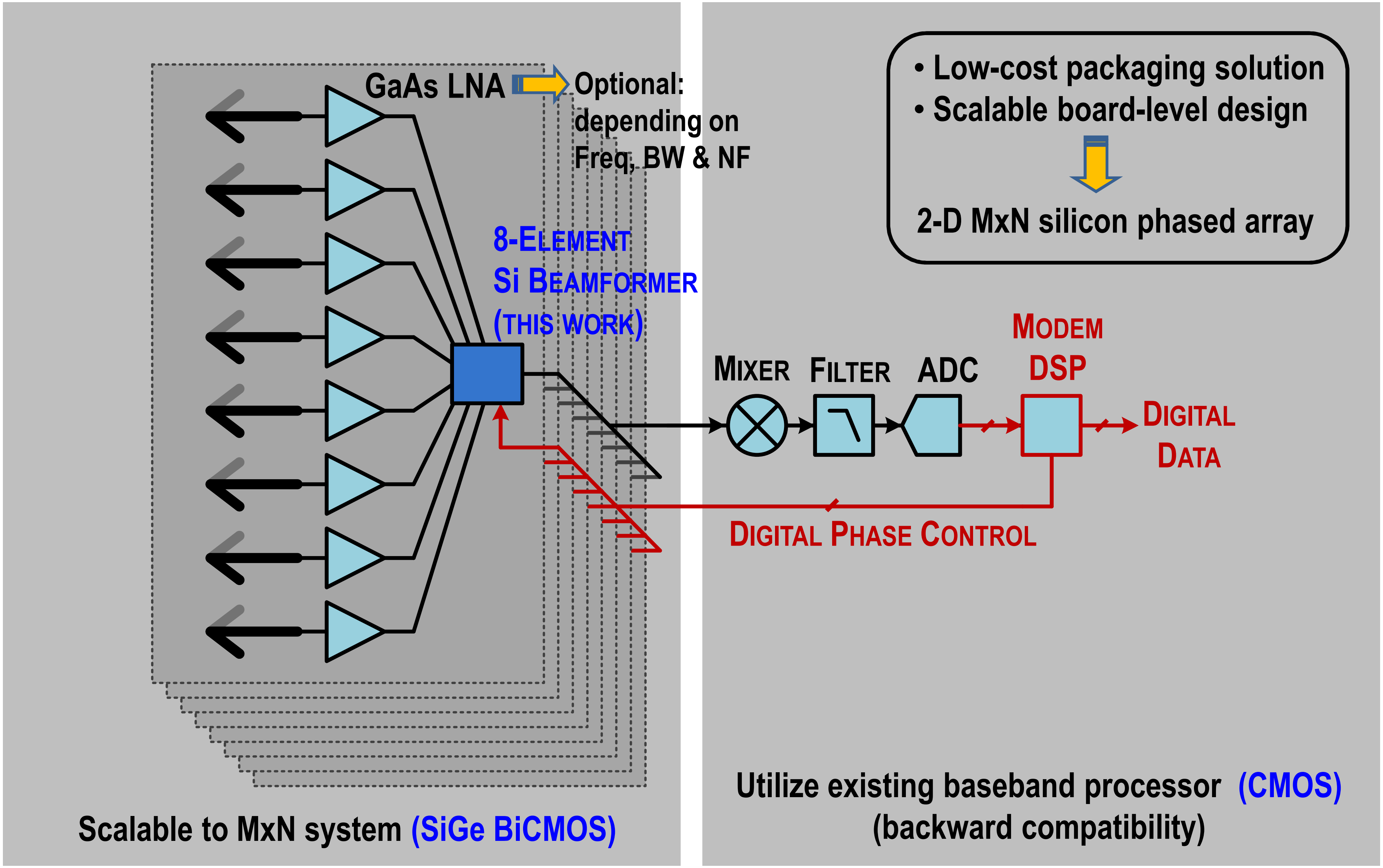
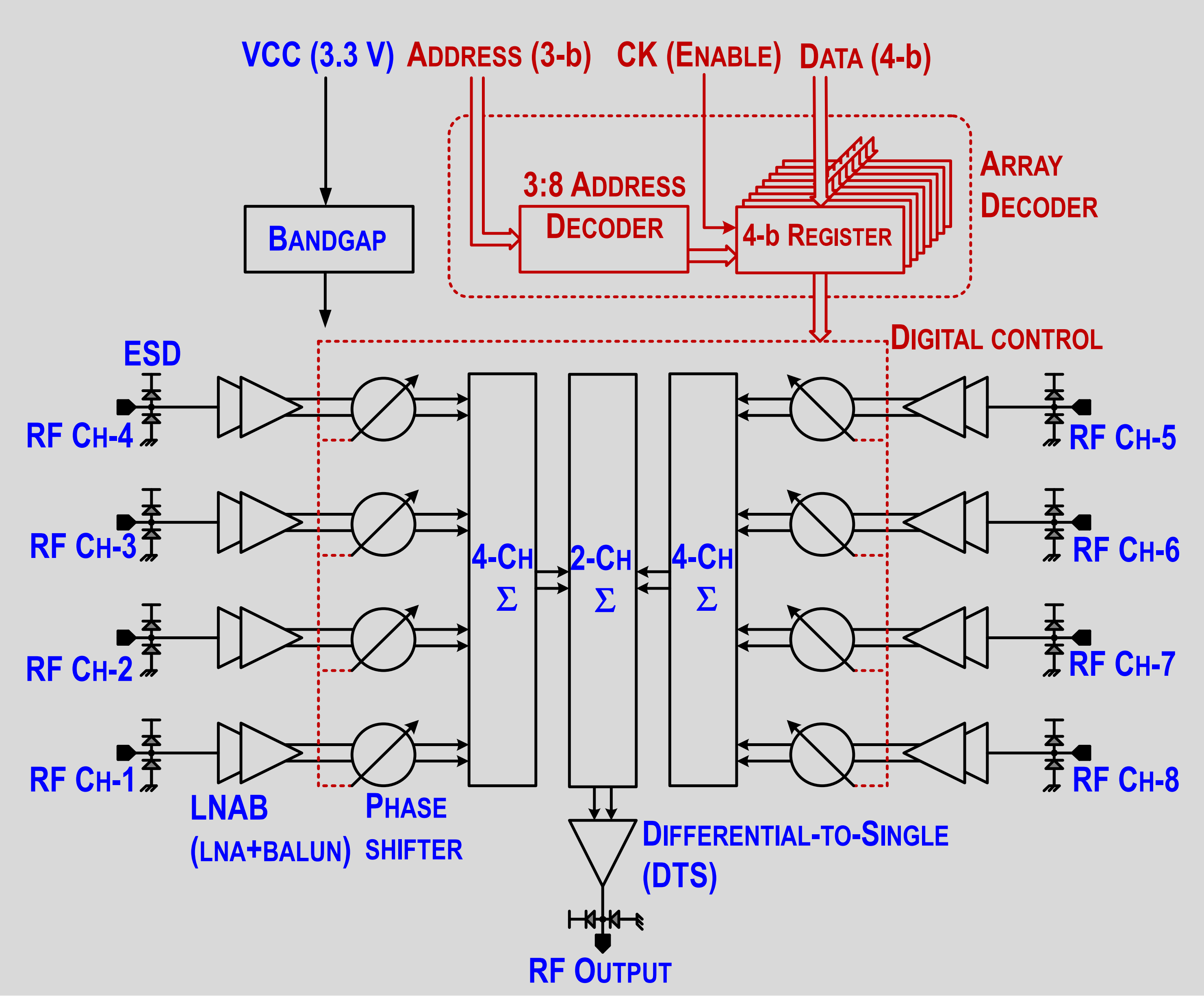


8-element phased-array (6-18 GHz, scalable array)

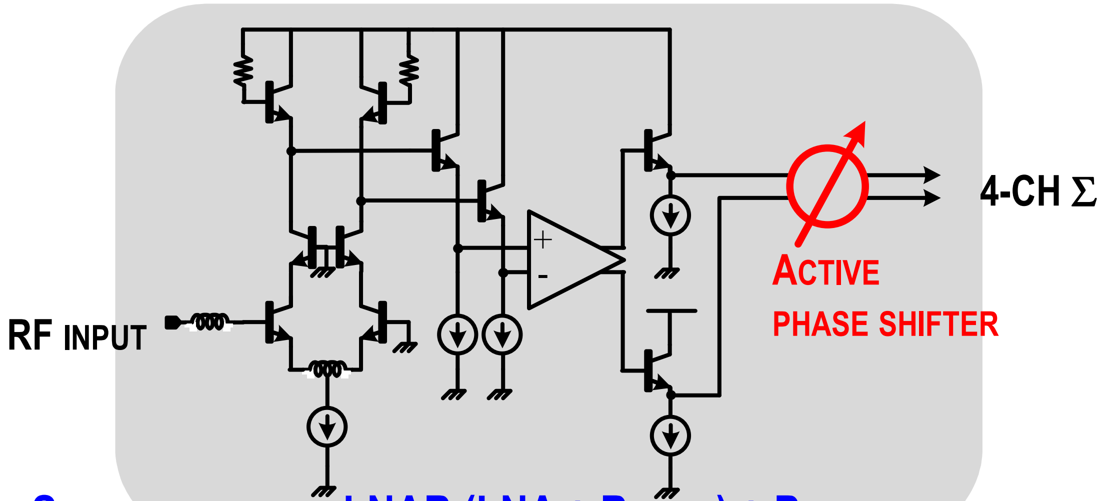


8-element phased-array (6-18 GHz, architecture)



- Integrate 8-CHs in SiGe
- Integrate "RF + DIGITAL"
- 4-bit active phase shifter
- 2-step signal combining (active adders)
- ESD protection (3kV, 2A)

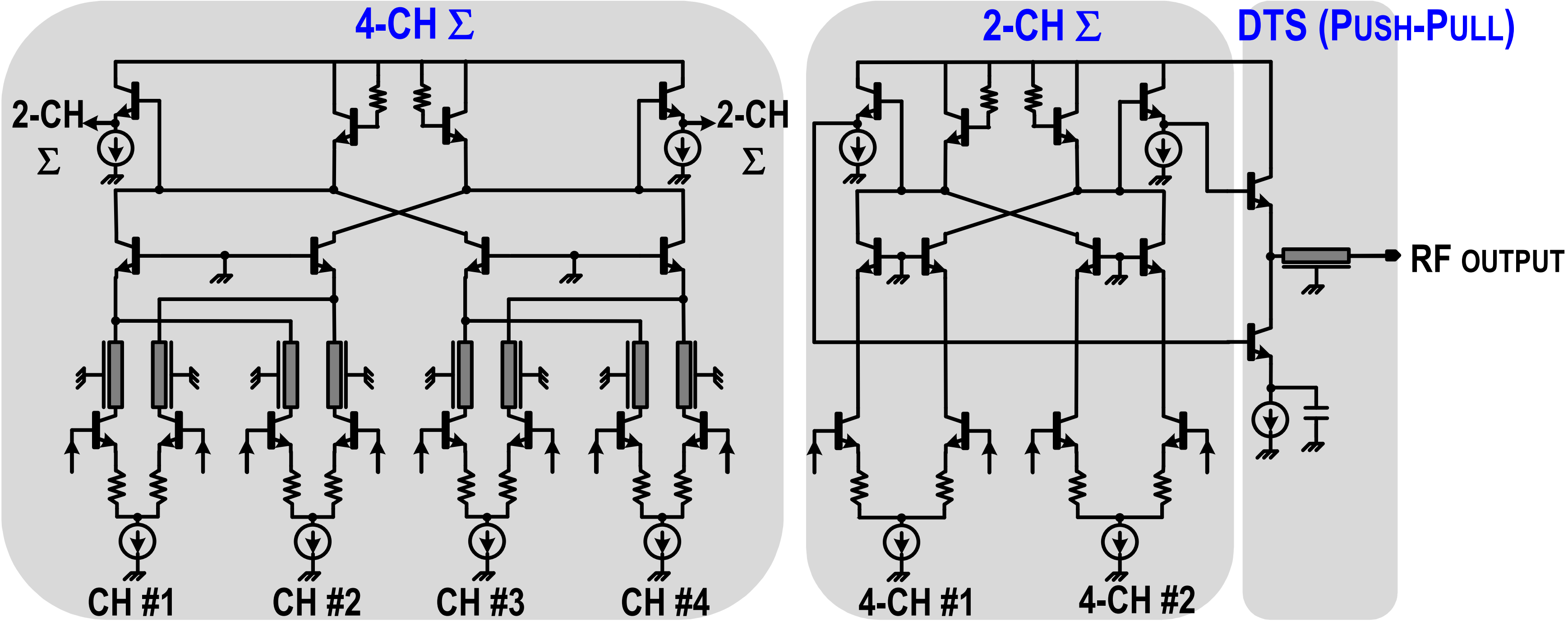
8-element phased-array (6-18 GHz, schematics)



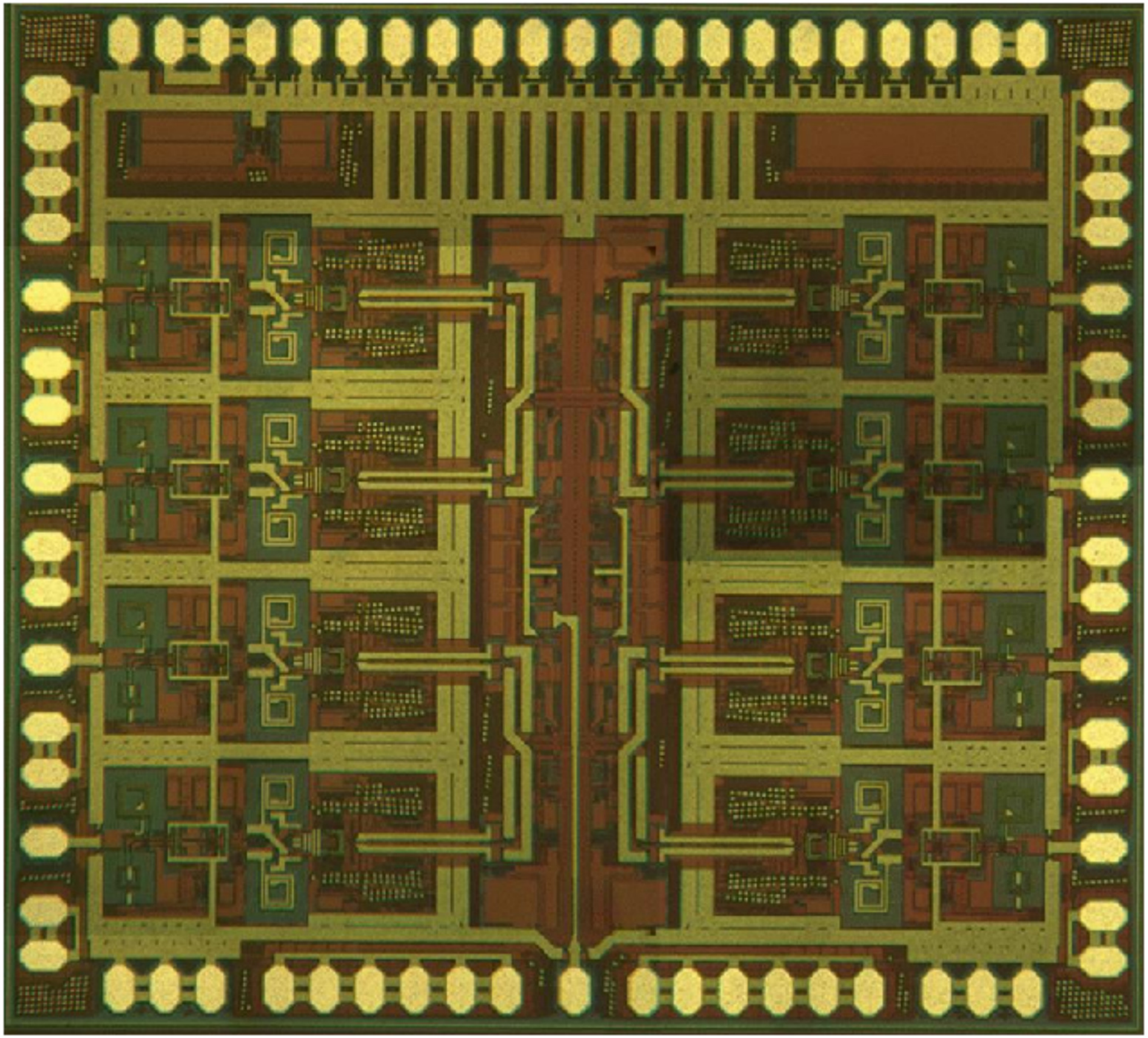
SINGLE CHANNEL: LNAB (LNA + BALUN) + PHASE SHIFTER

- Emitter-coupled diff-pair
- Single-to-differential conversion
- L-C input matching
- 2nd–stage diff amp: CMRR

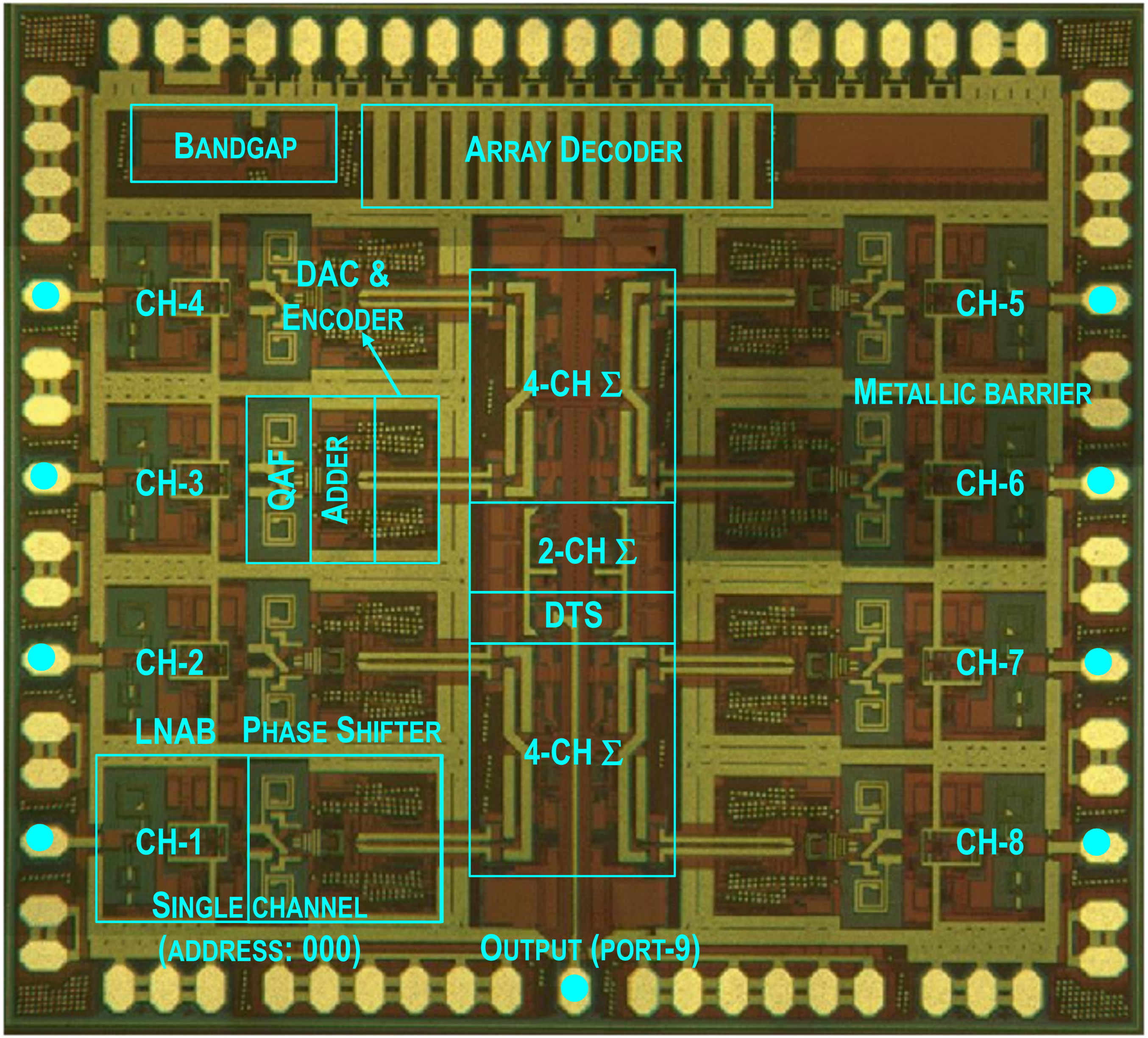
- Signal -Σ in current domain
- Binary fashion signal -Σ
- Wideband signal-Σ
- NMOS-based push-pull



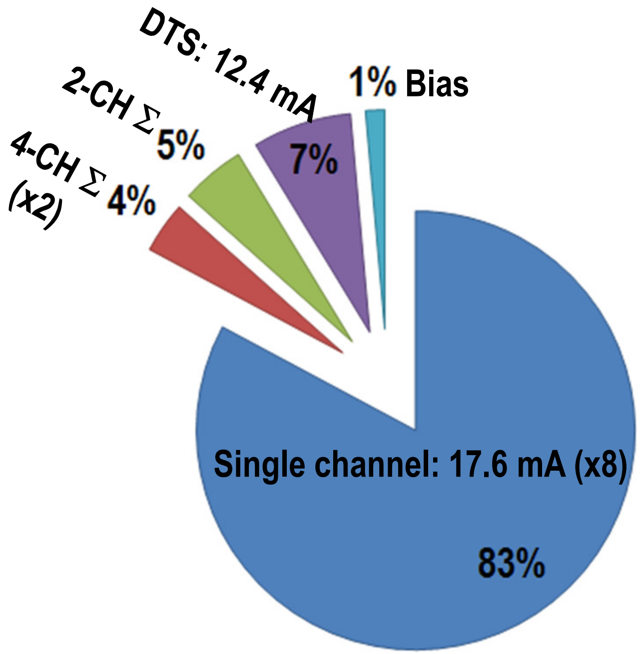
8-element phased-array (6-18 GHz, chip photo)



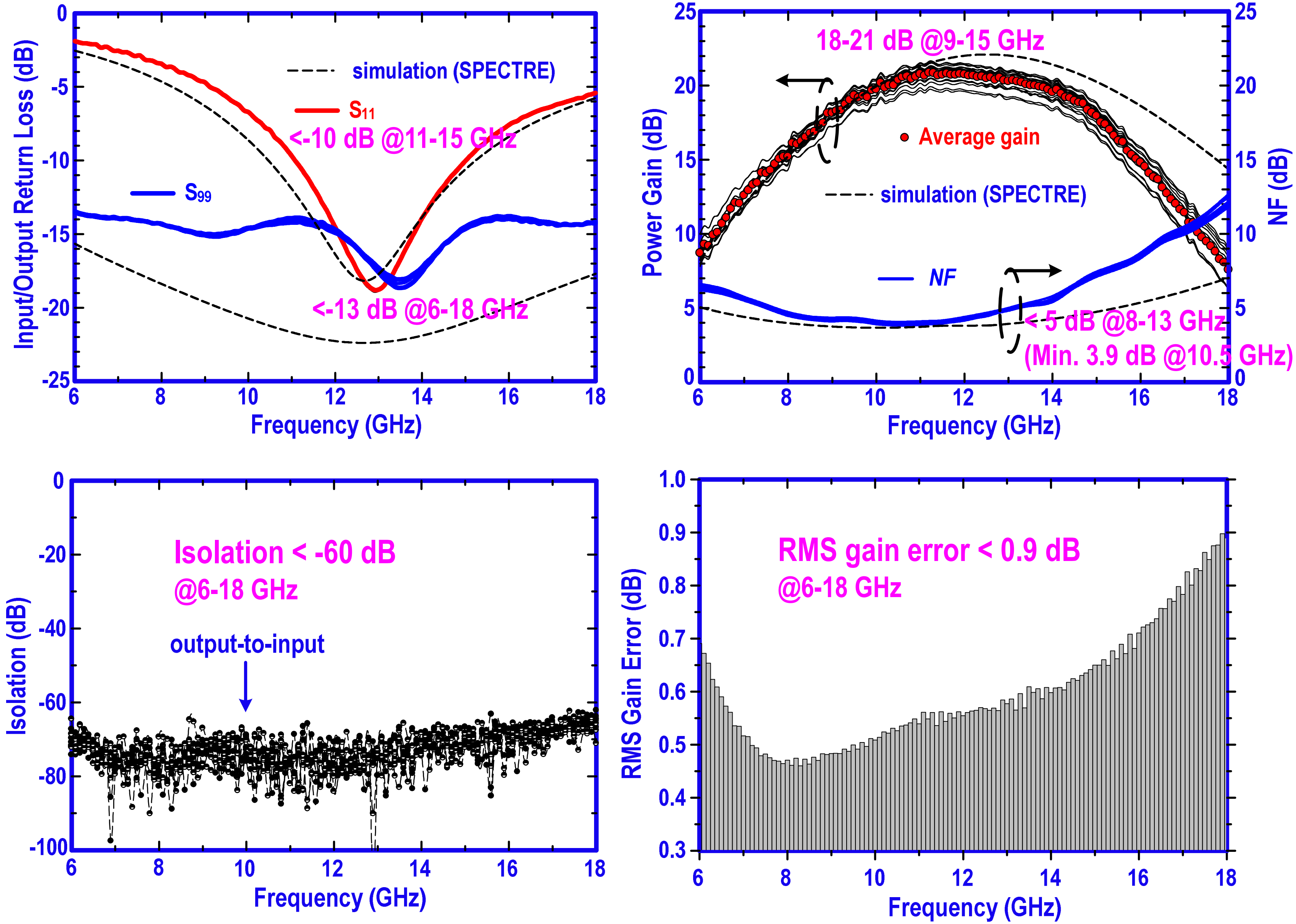
8-element phased-array (6-18 GHz, chip photo)



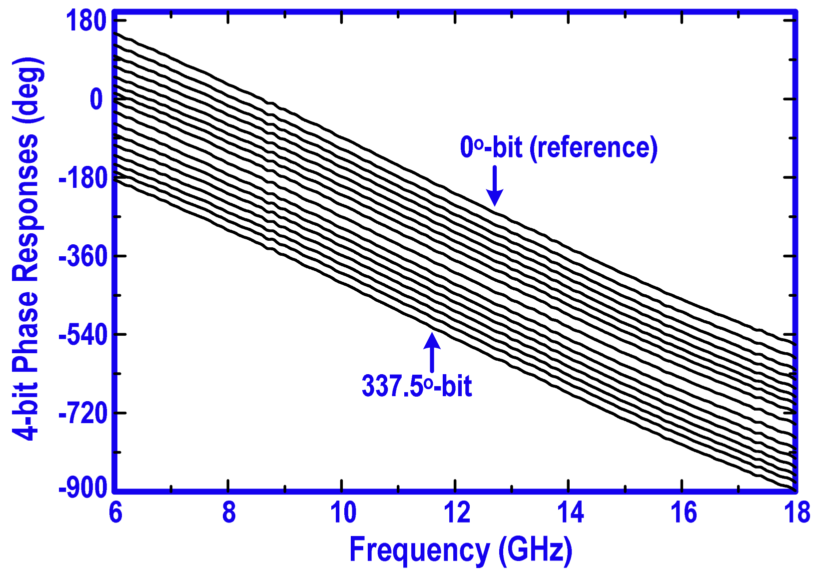
- 0.18-µm SiGe BiCMOS (Jazz SiGe120, 1P6M, f_T=150 GHz)
- Area = 2.2 x 2.4 mm^2
- Near perfect corporate-feed layout (E-length btw any input to output is identical)
- Metallic barrier: max CH-CH isolation
- V_{CC}=3.3 V, I_{total}=170 mA (561 mW, Active-Σ < 10%)

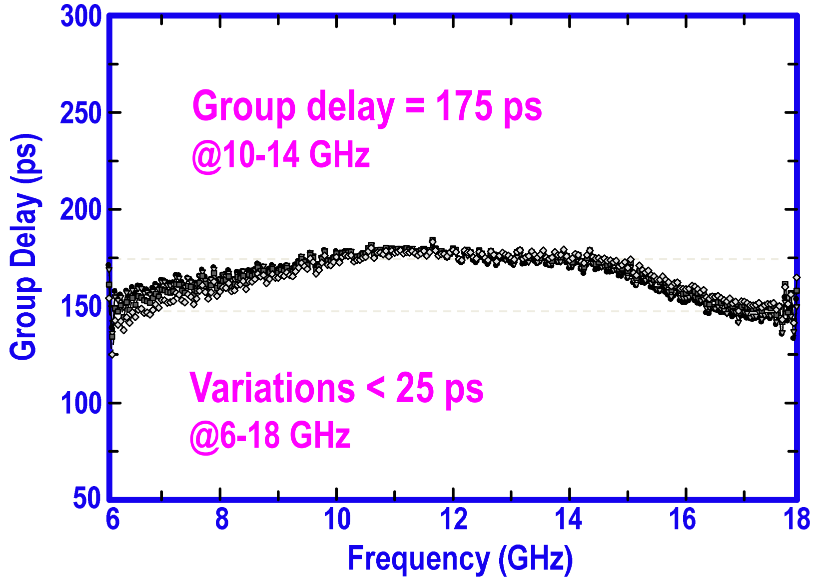


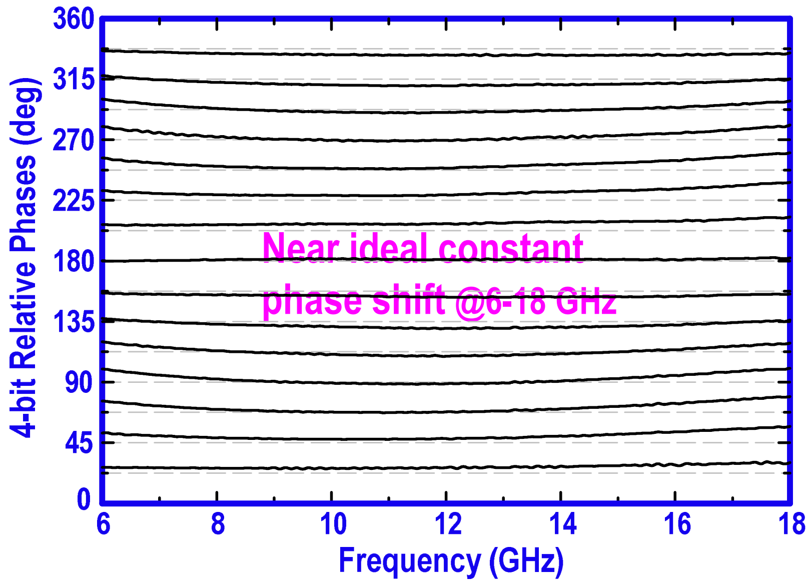
8-element phased-array (6-18 GHz, gain, NF, matching)

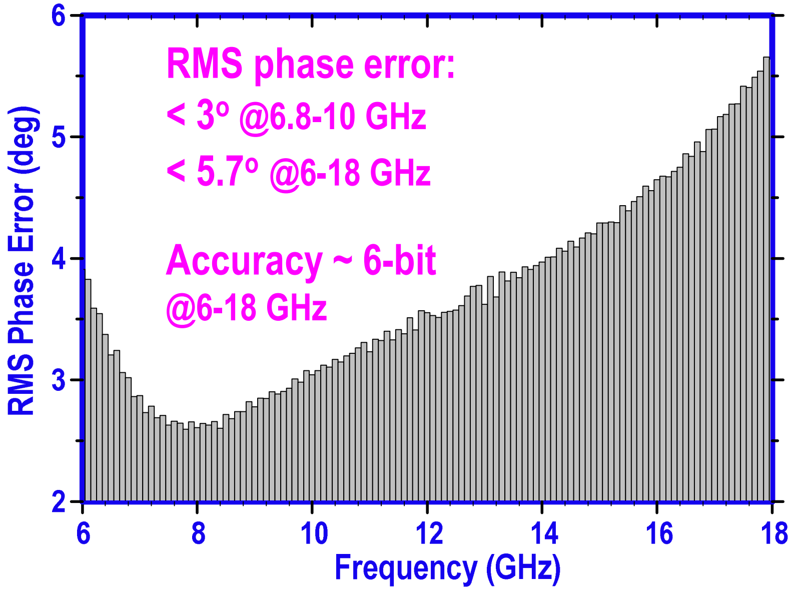


8-element phased-array (6-18 GHz, phase, group delay)

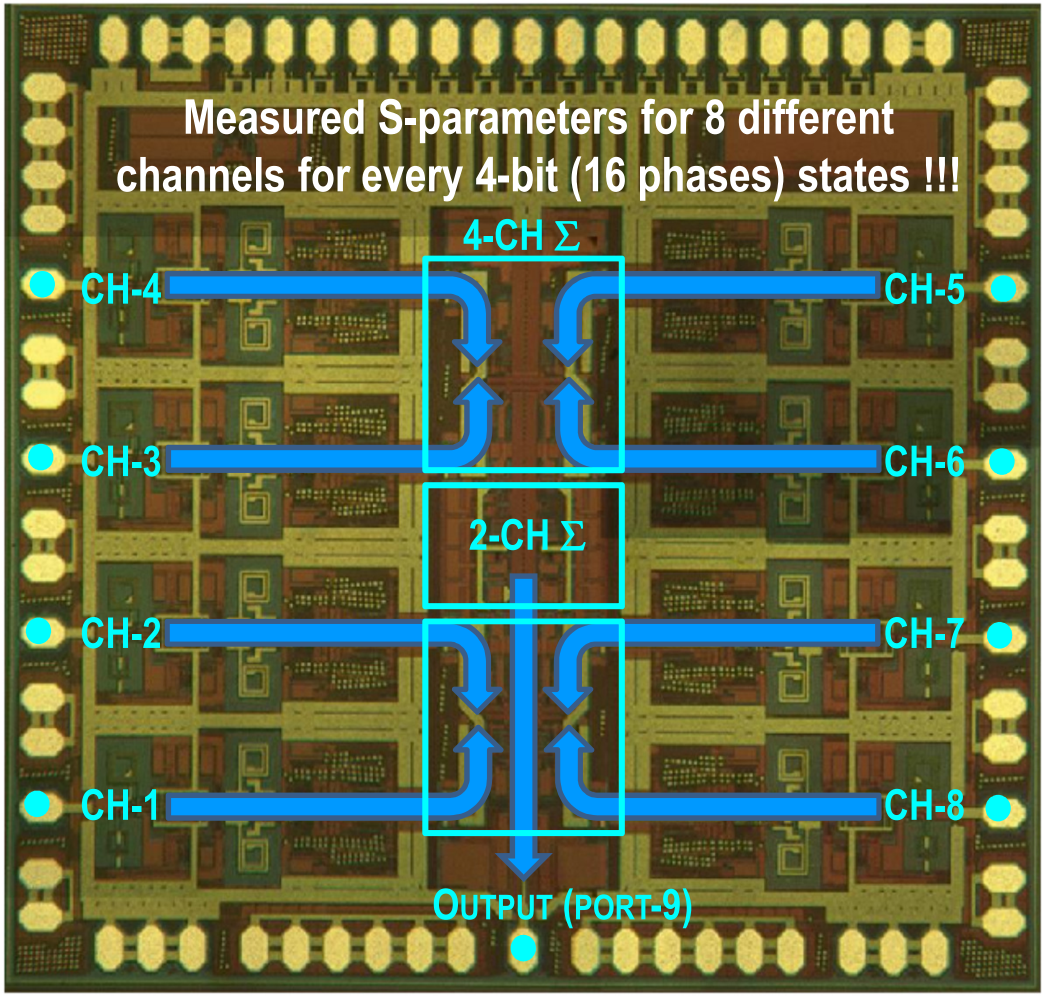


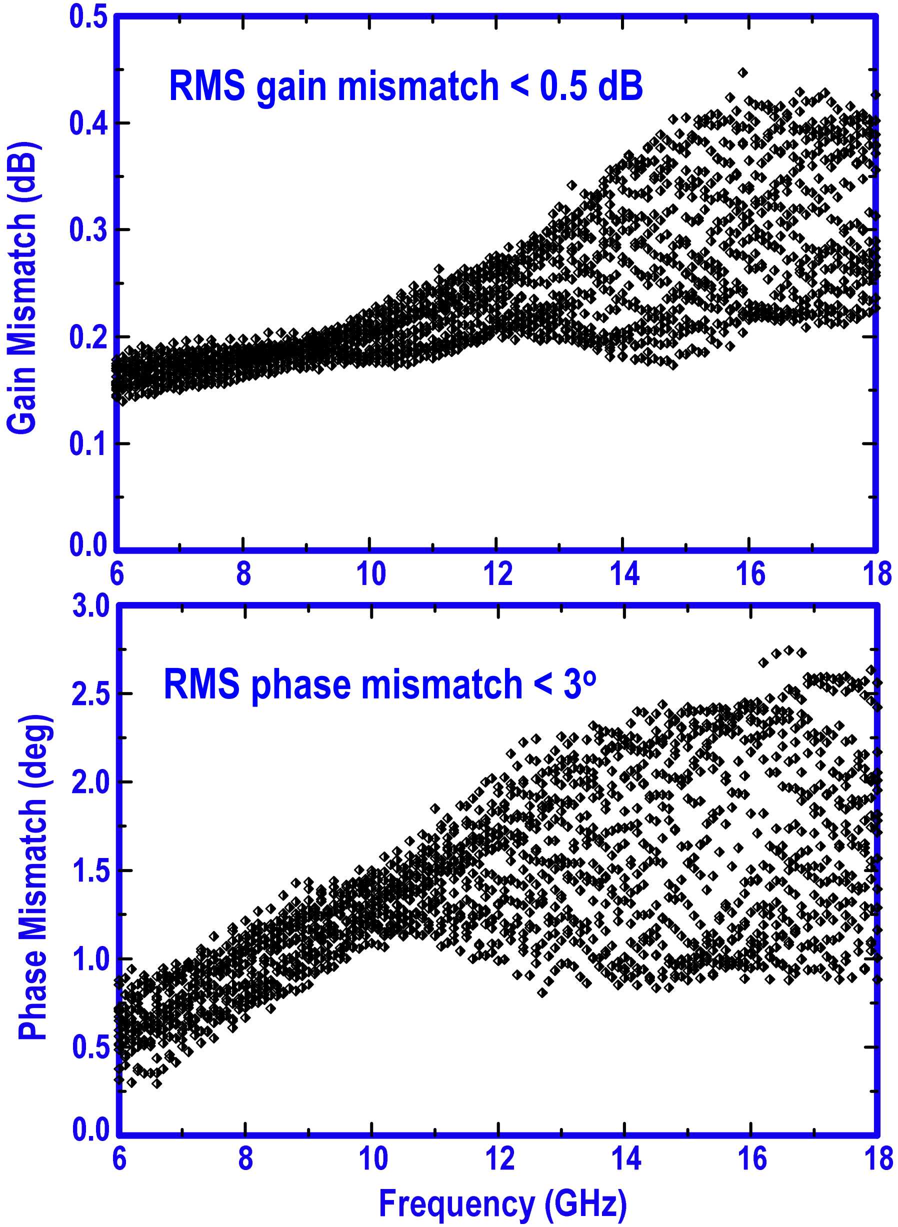






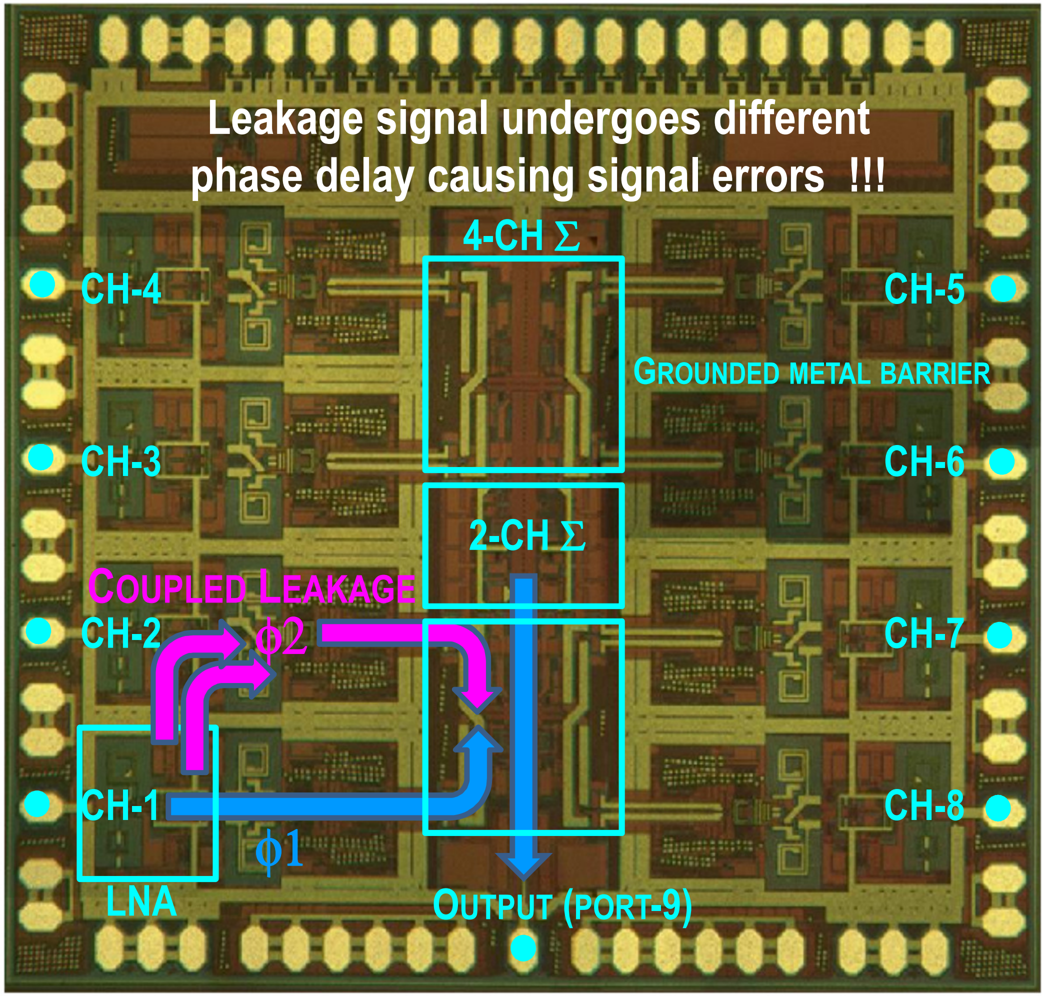
8-element phased-array (6-18 GHz, ch-to-ch variation)

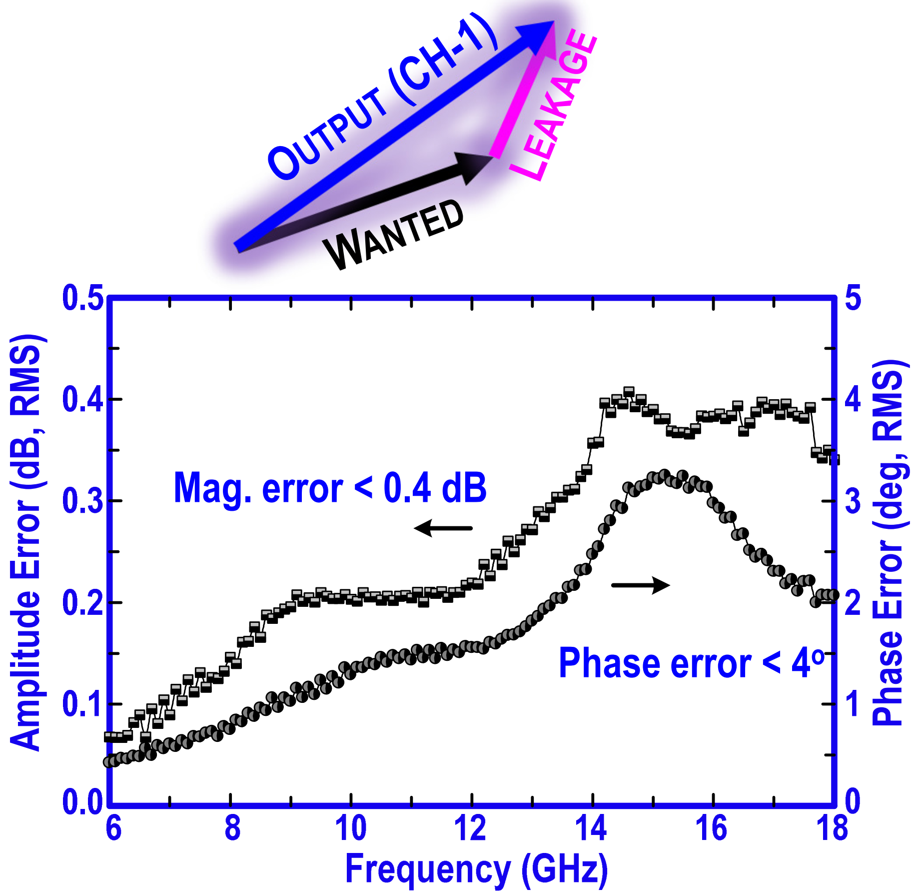




- Comparison of 128 S-Parameters
  = 8 (channels) x 16 (4-bit phases)
- Excellent matching between array elements
  → Major benefit in the on-chip integration

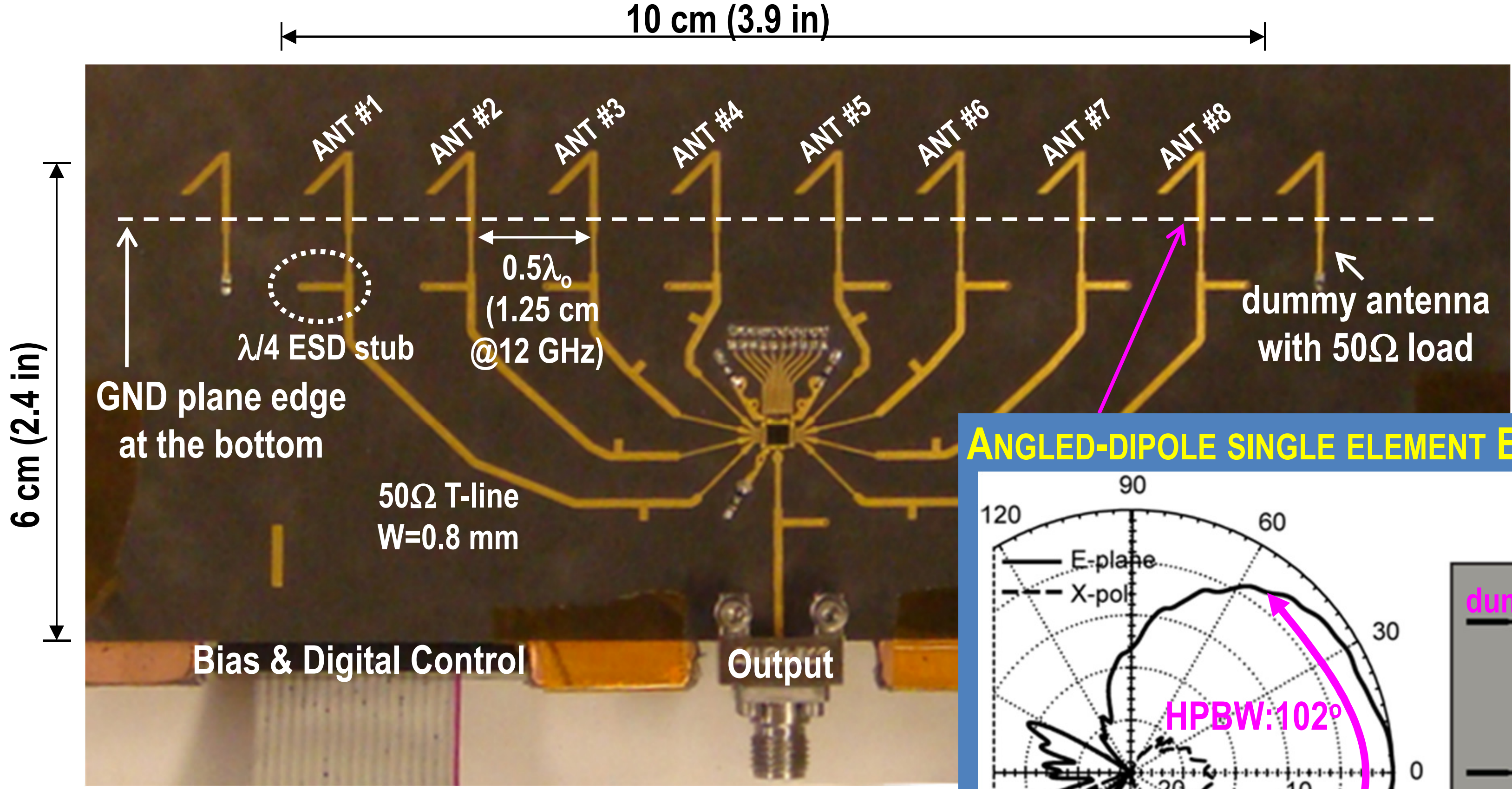
8-element phased-array (6-18 GHz, ch-to-ch coupling)



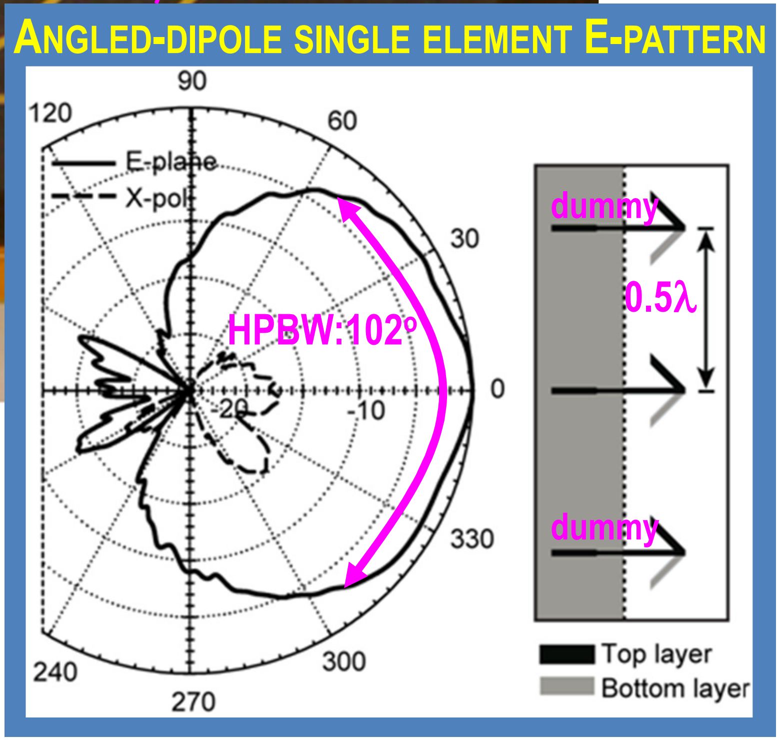


- Coupling causes amplitude & phase errors which could be serious in silicon
- Measured errors are negligible due to high isolation layout, e.g. metallic barrier

8-element phased-array (6-18 GHz, chip-on-board, angled-dipole)



Rogers RT5880 Teflon substrate (ε_r=2.2, h=10 mils)



ANGLED-DIPOLE ANTENNA:

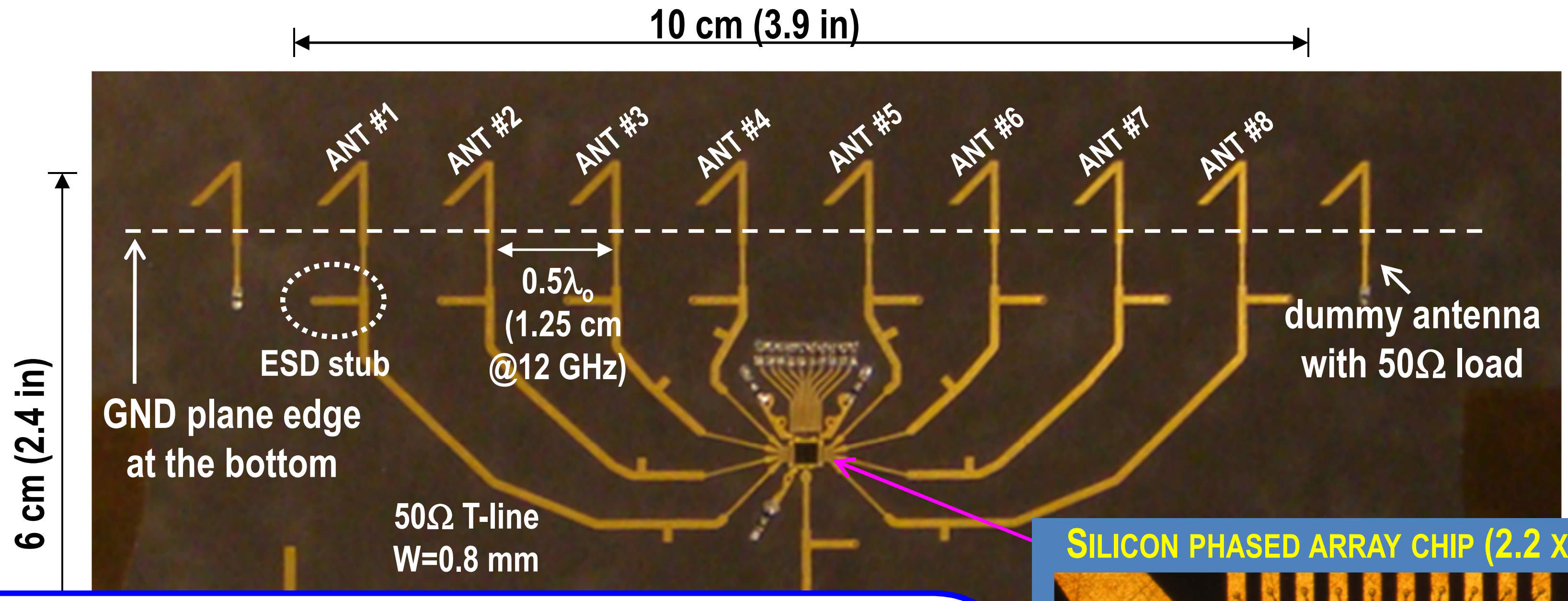
Wider beam width, Lower mutual coupling , Wideband S11

HPBW: 102°, S11<-10 dB @10.5-14 GHz, S21<-17 dB

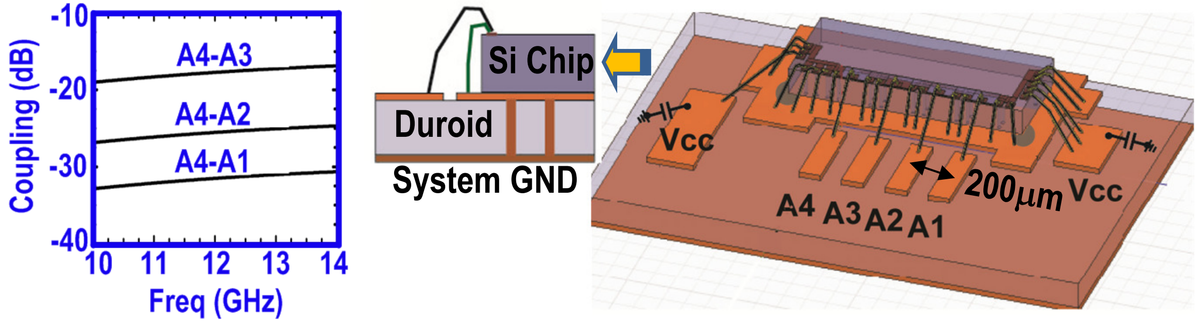
Scan angle: +/- 60° w/ 4dB drop in element factor

Ref: Y. A. Atesal, B. Cetinoneri, K.-J. Koh, G. M. Rebeiz, "X/Ku-Band 8-Element Phased Arrays Based on Single Silicon Chips", 2010 IMS, May 2010

8-element phased-array (6-18 GHz, chip-on-board, chip mounting)

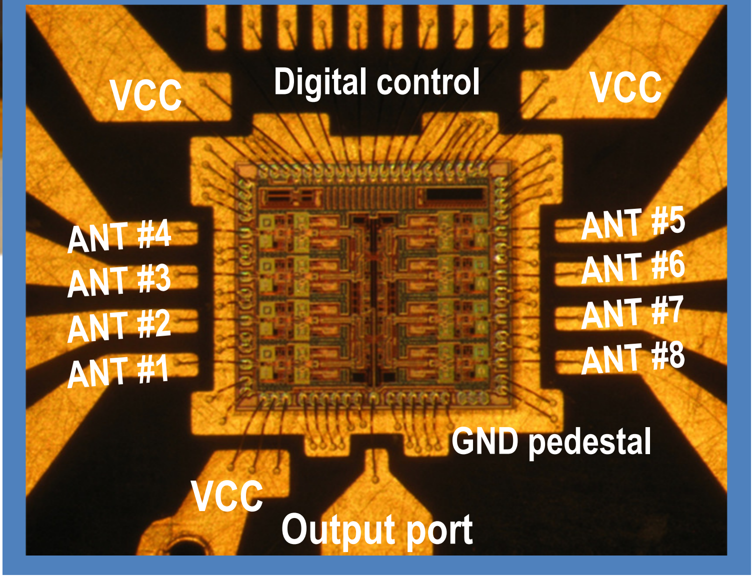


Bondwire & Coupling simulation with HFSS



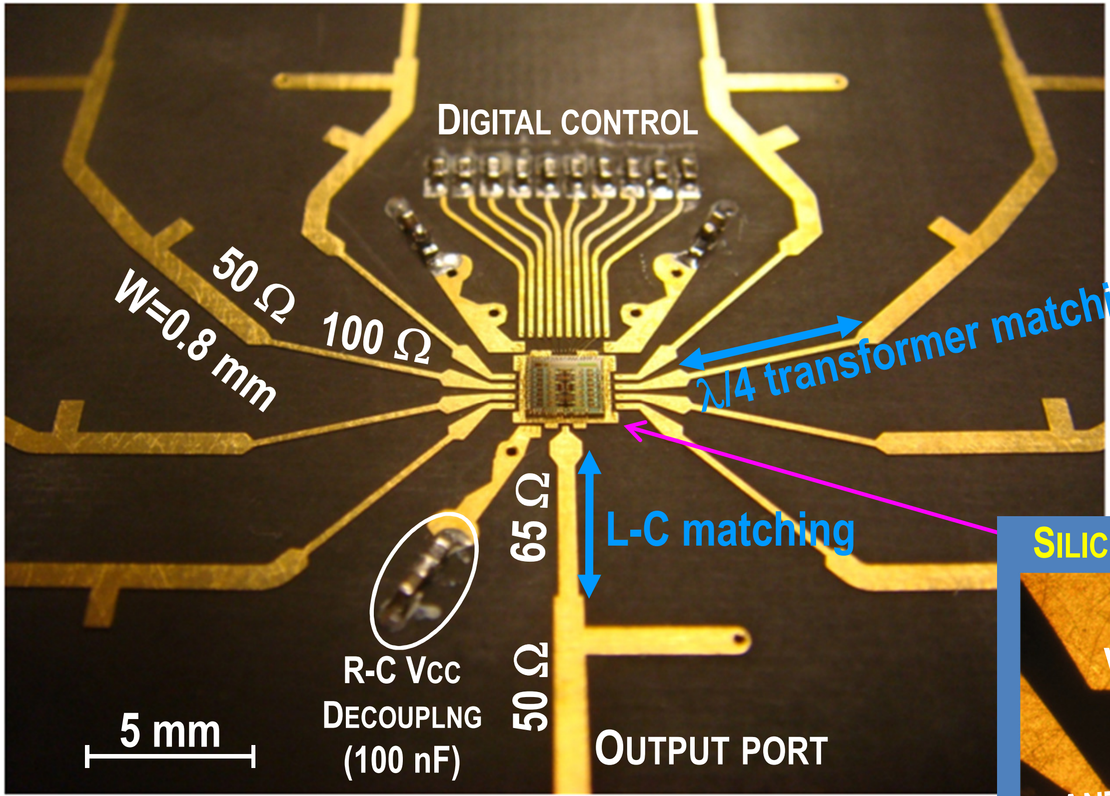
Worst-case coupling < -17 dB, bondwire inductance: 0.5 nH

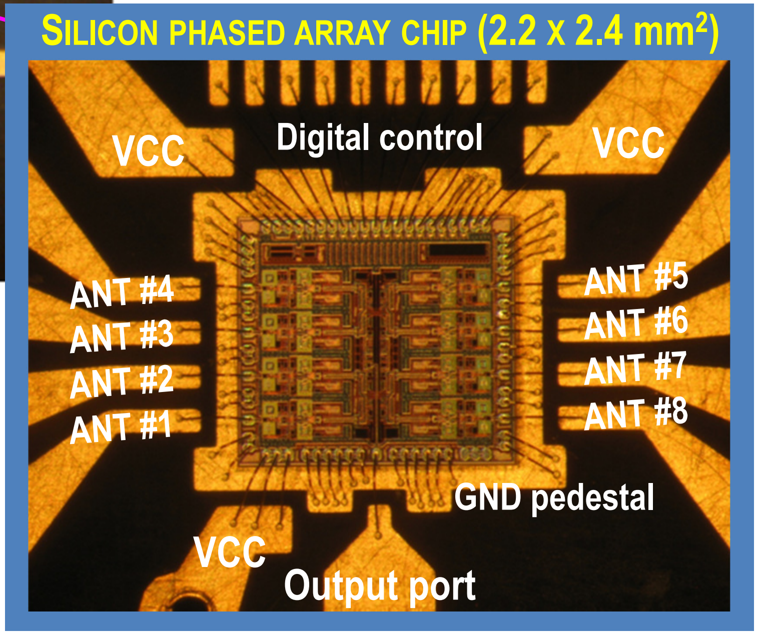
Silicon phased array chip (2.2 x 2.4 mm²)

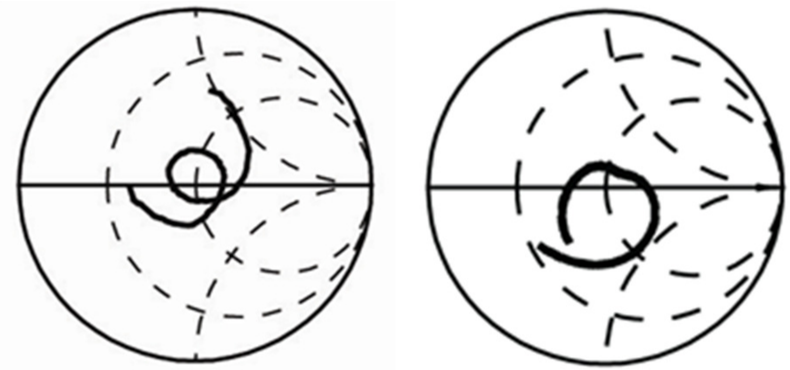


Ref: Y. A. Atesal, B. Cetinoneri, K.-J. Koh, G. M. Rebeiz, "X/Ku-Band 8-Element Phased Arrays Based on Single Silicon Chips", 2010 IMS, May 2010

8-element phased-array (6-18 GHz, chip-on-board, z-matching)



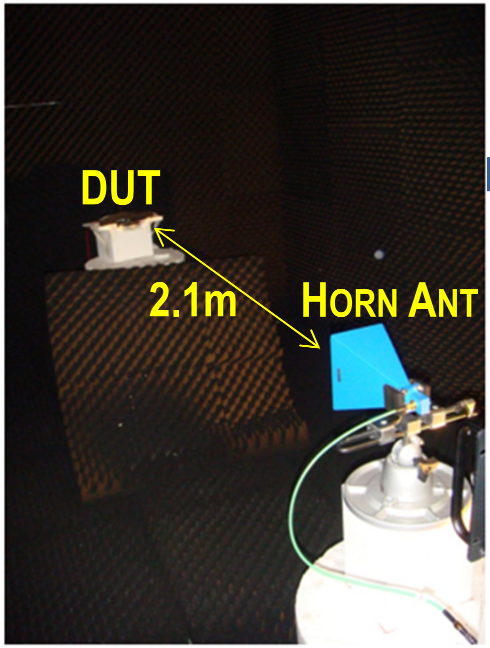


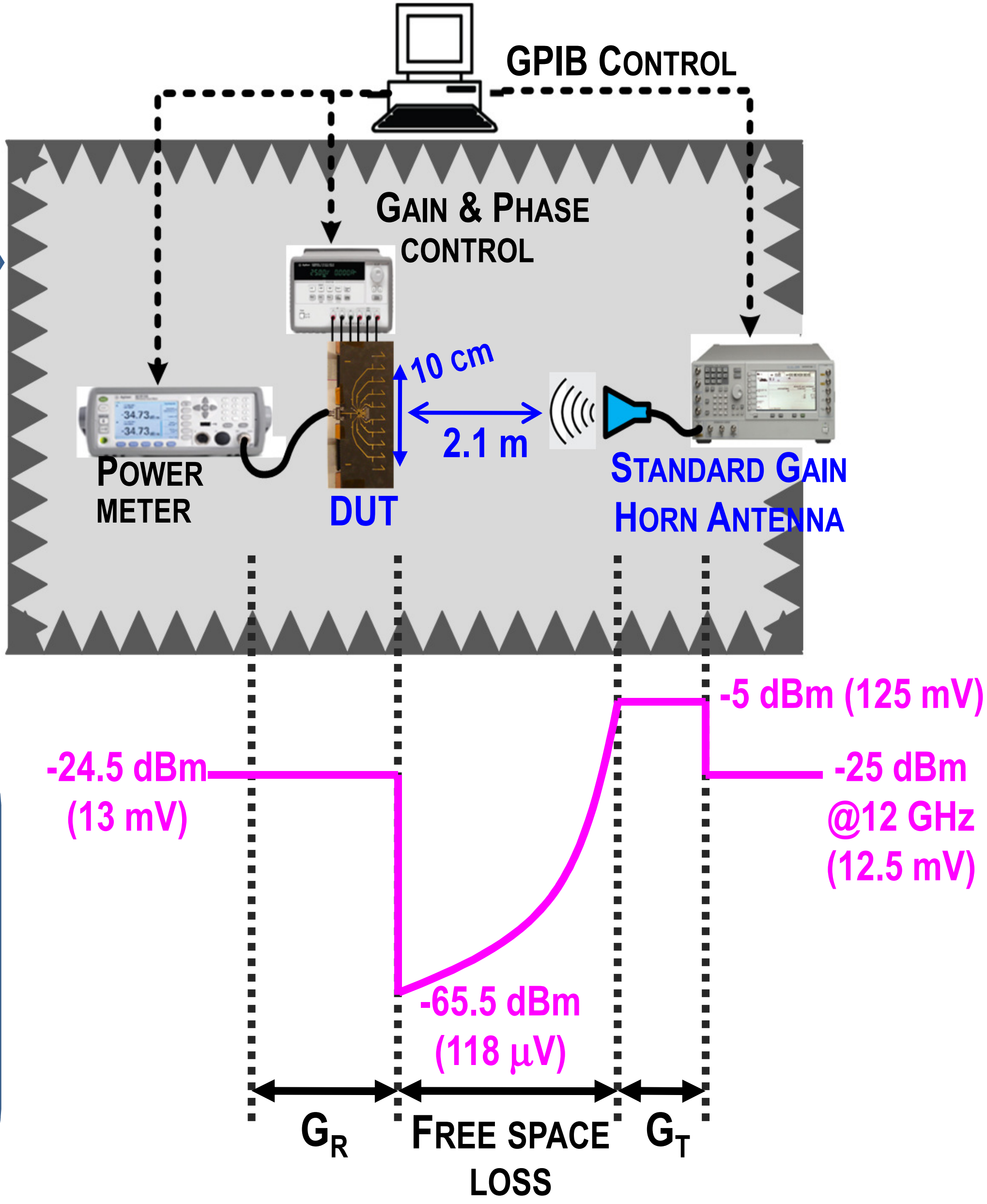


S_{11} < -10 dB @ 10-14 GHz S_{22} < -10 dB @ 8.5-13.5 GHz

8-element phased-array (6-18 GHz, board measurement setup)

ANECHOIC ANTENNA CHAMBER





Friis TRANSMISSION EQUATION

$$\frac{P_R}{P_T} = \underbrace{G_T}_{\text{Horn ANT gain}} \times \underbrace{\left(\frac{\lambda}{4\pi \cdot R}\right)^2}_{\text{Free space path loss}} \times \underbrace{G_R}_{\text{Phased array gain}}$$

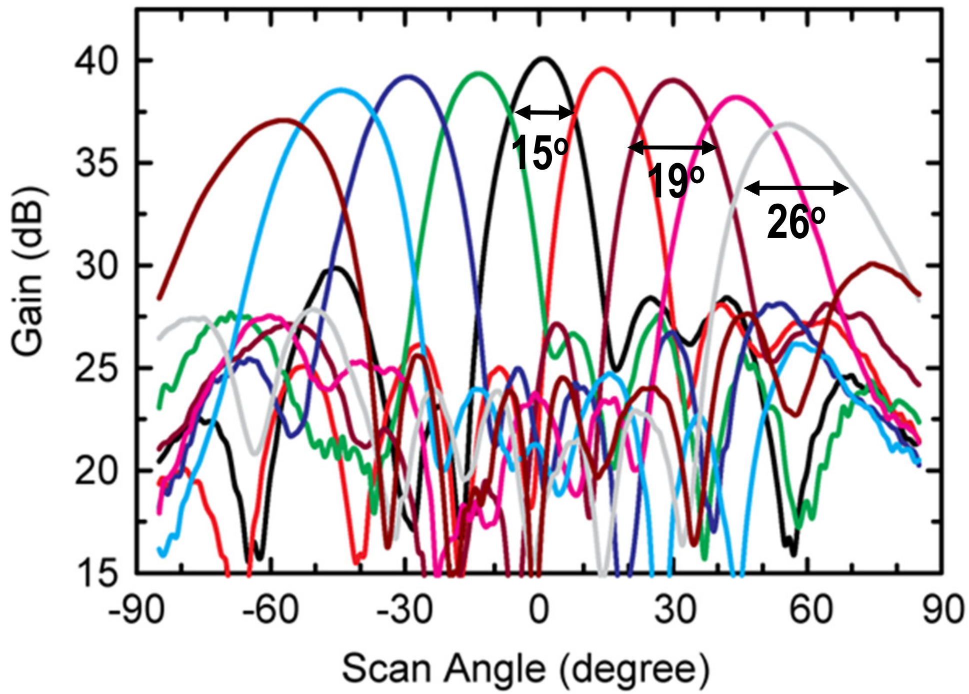
Horn ANT gain = 20 dB

Free space path loss = -60.5 dB
R: 2.1 m
λ: 2.5 cm
@12 GHz

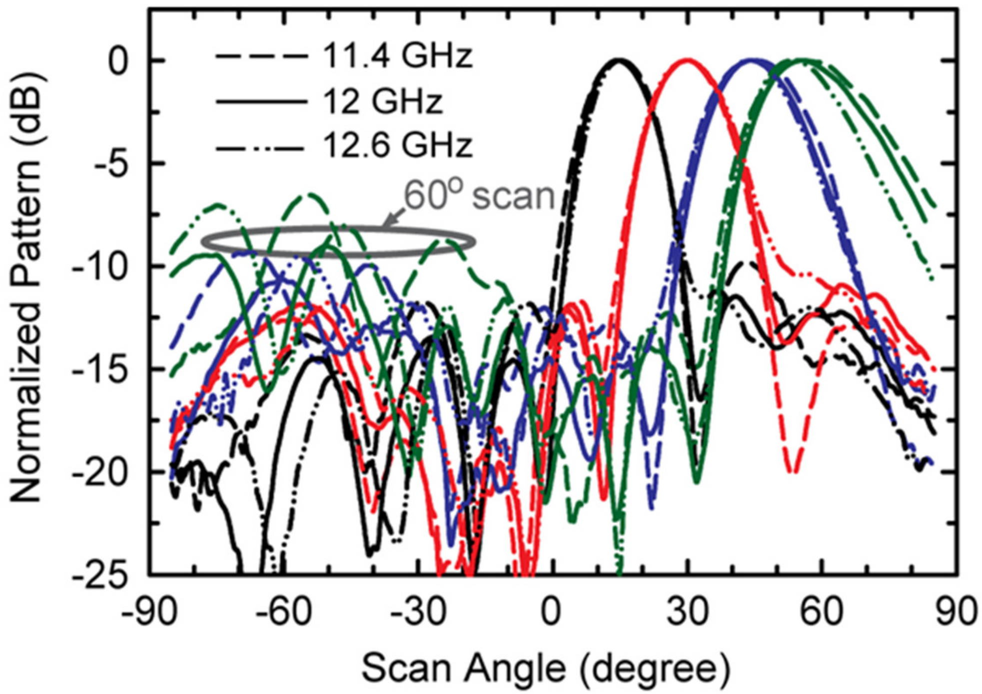
Phased array gain = 41 dB
Channel gain (20 dB)
Array factor (18 dB)
Antenna gain (3 dB)

8-element phased-array Rx (6-18 GHz, board measurement)

MEASURED PATTERN @12 GHz



MEASURED PATTERN @11.4-12.6 GHz

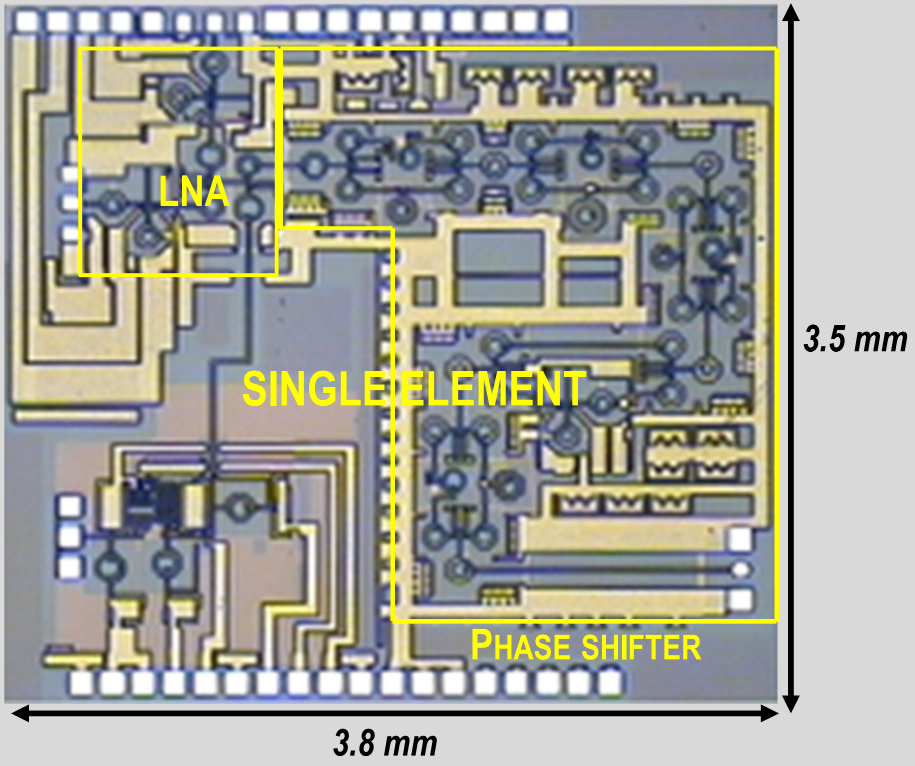


- Scanned from -60° to 60°
- Element factor causes 3-4 dB drop at 60°
- HPBW: 15° @0°-scan, 19° @30°-scan, 26° @60°-scan
- Excellent agreement with simulations

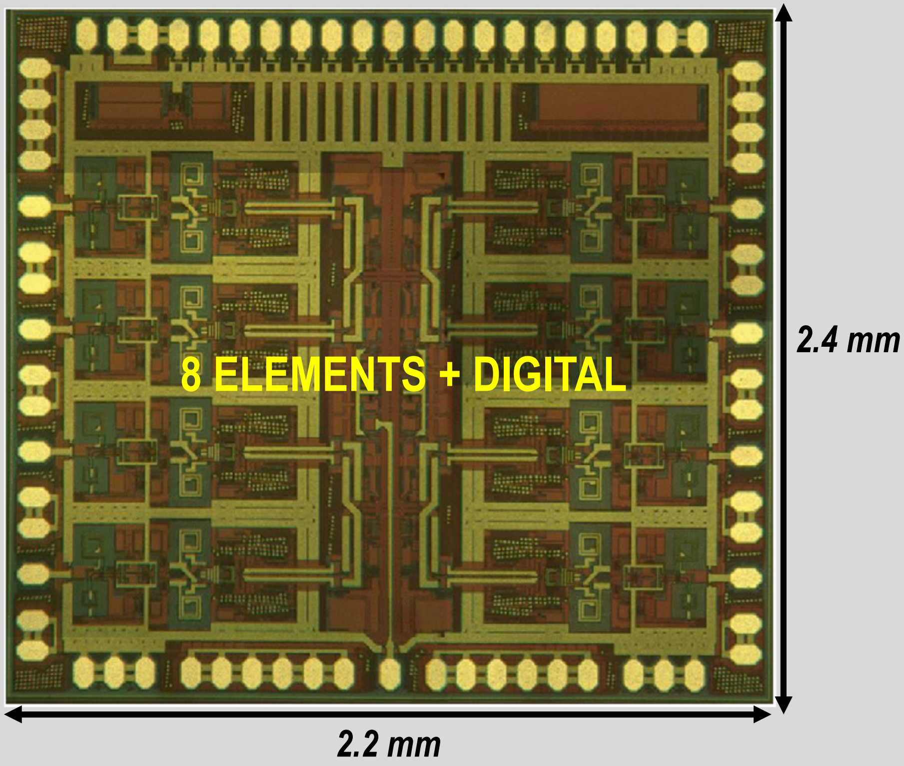
- No-true-time delay on each element
- Slight beam walk @ 60°- scan angle
- Instantaneous BW limited to 11.4-12.6 GHz (Δ=1.2 GHz, 10%)

First system-level (w/ antenna) demo of an X-band array based on a single silicon chip !

Area comparison: single vs. 8-array



Ref: Comeau etal (Georgia Tech), “A SiGe Receiver for X-Band T/R Radar Modules”, IEEE JSSC, Sept. 2008



Ref: K.-J. Koh etal, “An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18-µm SiGe BiCMOS Technology”, IEEE JSSC, June 2008

Integration (A=13.3 mm^2):
LNA + Phase shifter + bias c.k.t.
(single element: analog)

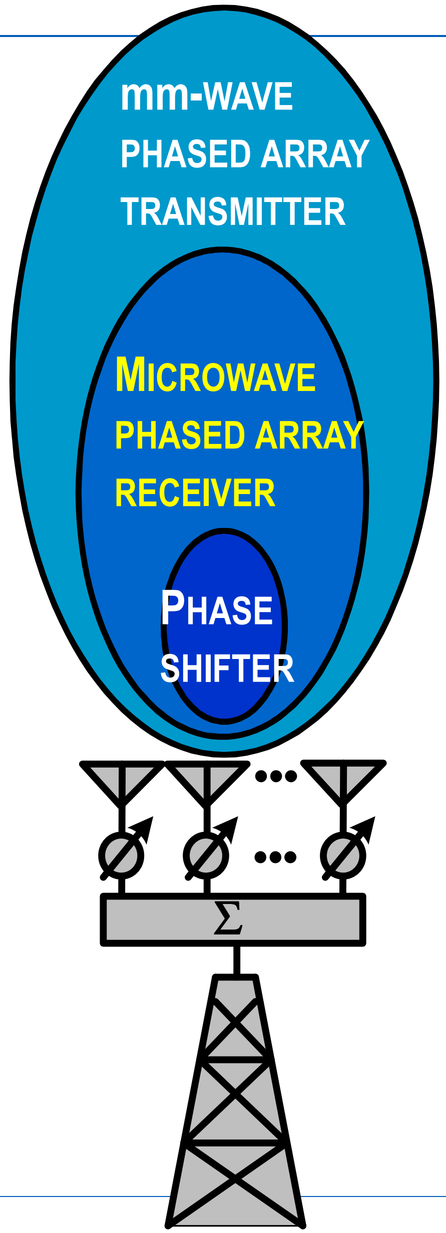
Just 40% area!

Compare

Integration (A=5.3 mm^2):
8 LNAs + 8 Phase shifters + bandgap
(8 elements: analog)
+
Array decoder (digital control)

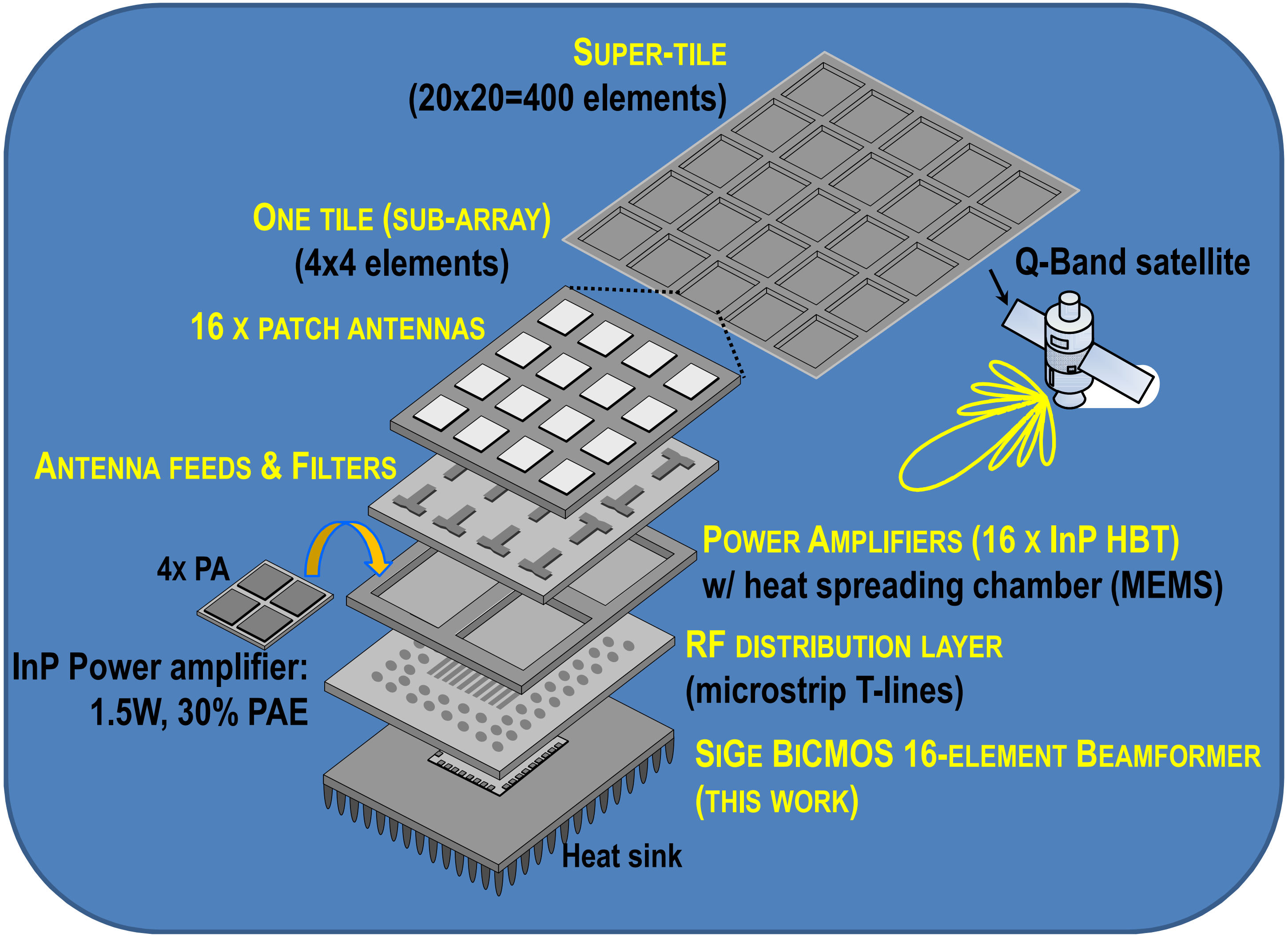
Outline

- Introduction
  - Discrete phased array: example
- Phase shifter design
  - Active phase shifter
  - Some comparisons with passive one
- **Phased array designs**
  - X-band receiver
  - **Q-band transmitter & receiver**
  - W-band & beyond
- Conclusion



16-element Q-band phased-array Tx (large array, 3-D integration)

PROJECT: DARPA SCALABLE MILLIMETER-WAVE ARRAY TECHNOLOGY (SMART, 2006-2008)



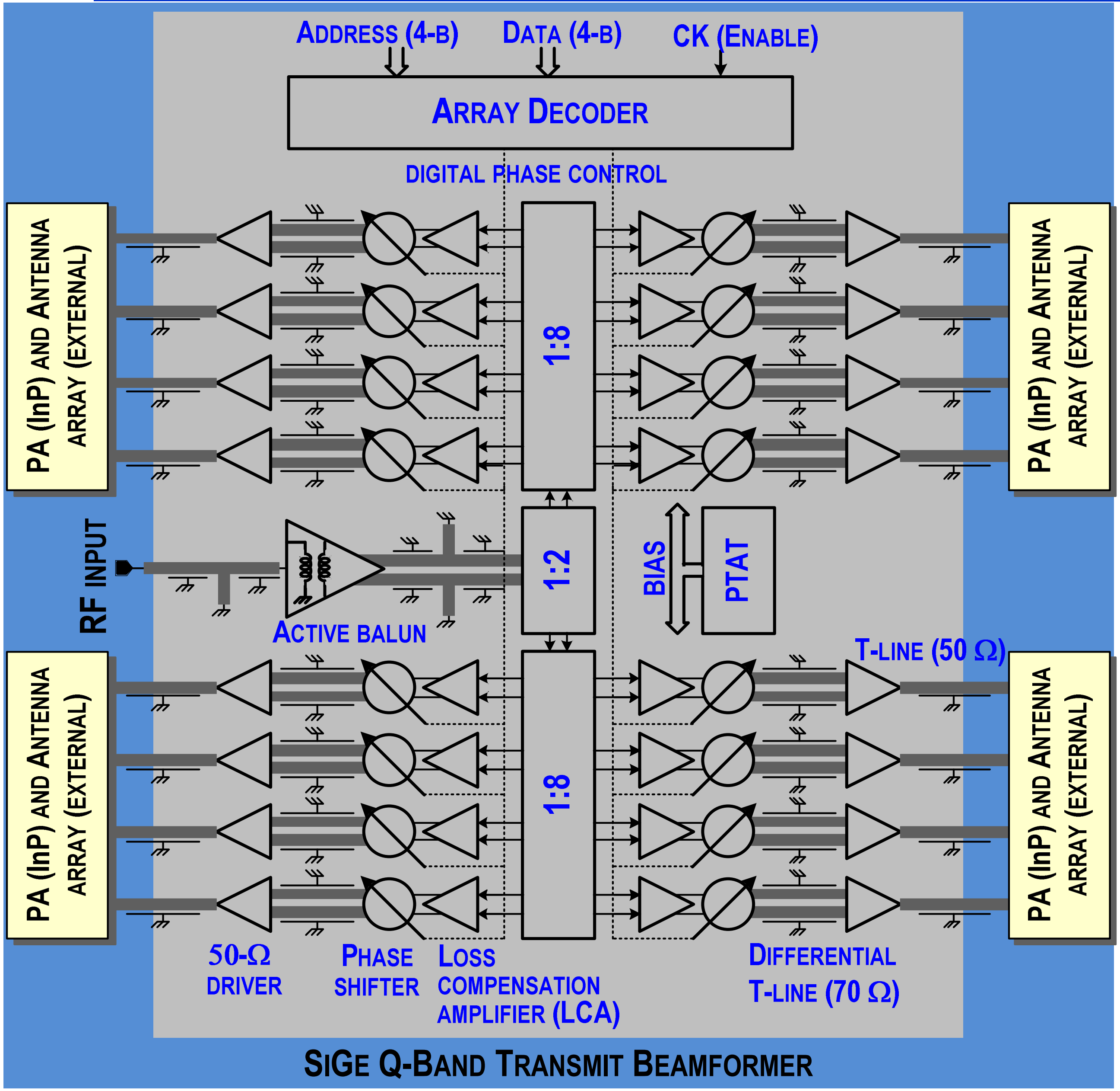
TILE-BASED 2-D LARGE ARRAY (20X20) CONSTRUCTION
ONE TILE (SUB-ARRAY): 4X4 ELEMENT, ONE SUPER-TILE: 5X5 TILES

- Q-band satellite comm. (43-45 GHz, $\lambda/2$=3.4 mm)
- Large array: 20x20 elements
- Microstrip antenna size = 3.4x3.4 mm^2
- Integrate 1 sub-array (4x4) in a single package (Area < 3x3 cm^2)

↓

Multi-layered integration in a single package

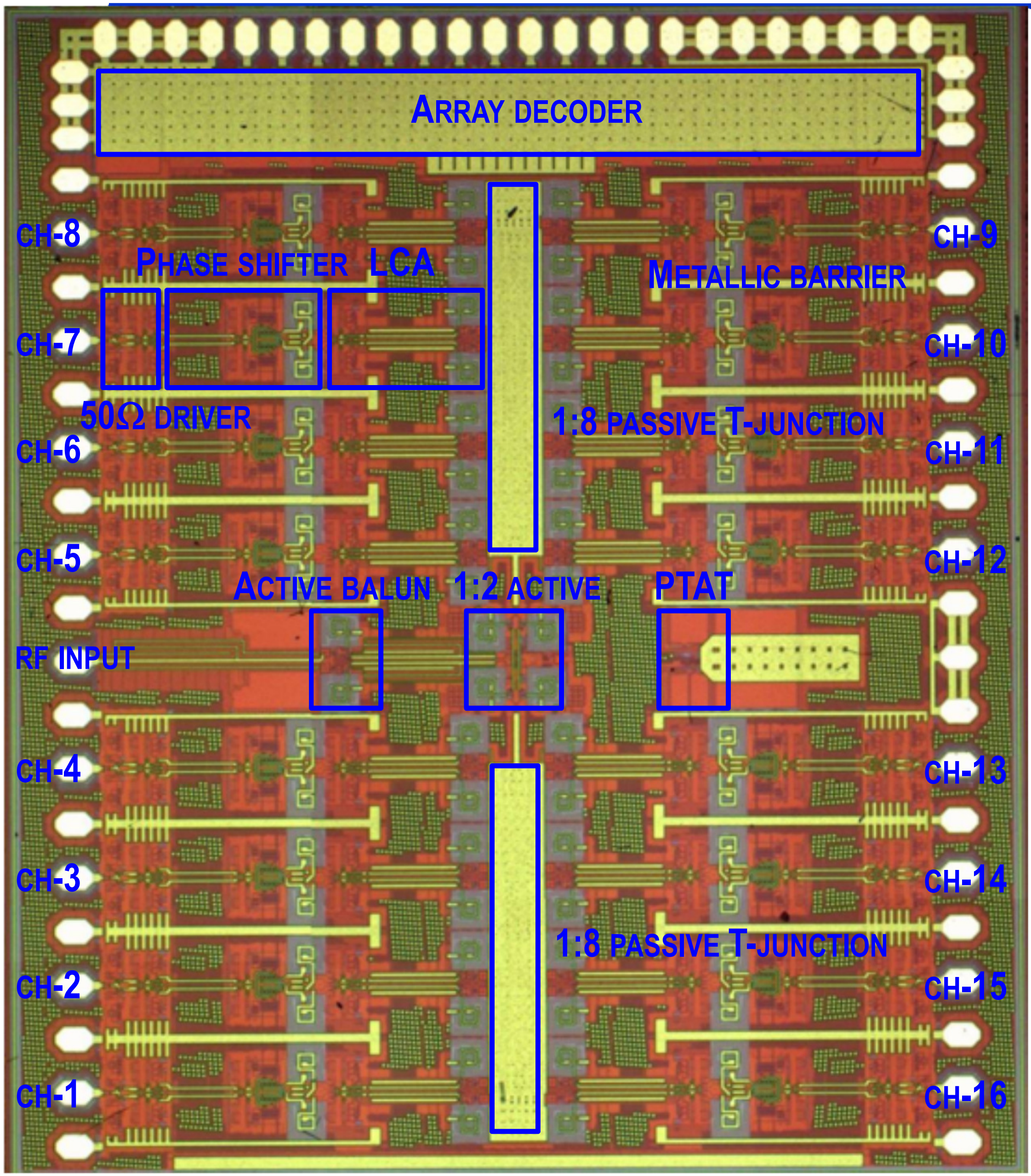
16-element Q-band phased-array Tx (44 GHz, architecture)



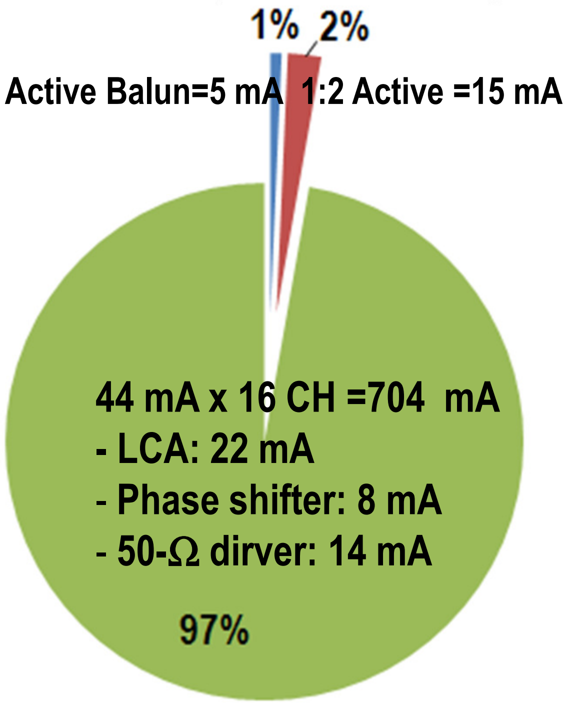
- 44 GHz satellite comm. application
- Integrate 16 elements (4x4)
- Corporate feed architecture
  - Active balun, 1:2 active, 1:8 passive
- Single channel elements
  - LCA: compensate 1:8 division loss
  - 4-bit active phase shifter
  - 50-Ω driver drives external PA
- Array decoder
  - control each channel independently

Ref: K.-J. Koh *etal*, "A Millimeter-wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18-µm SiGe BiCMOS Technology", IEEE JSSC, May 2009

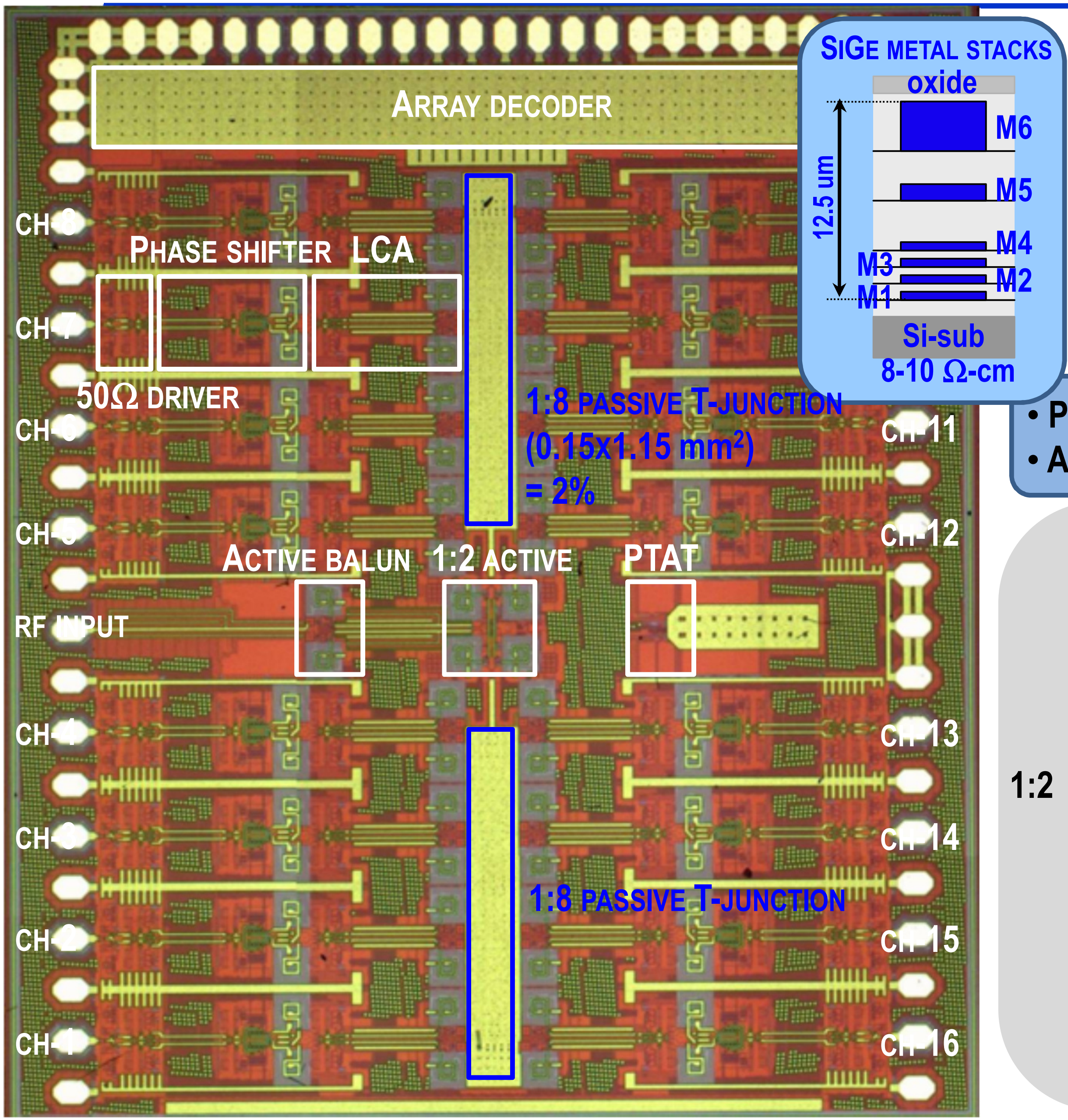
16-element Q-band phased-array Tx (44 GHz, chip photo)

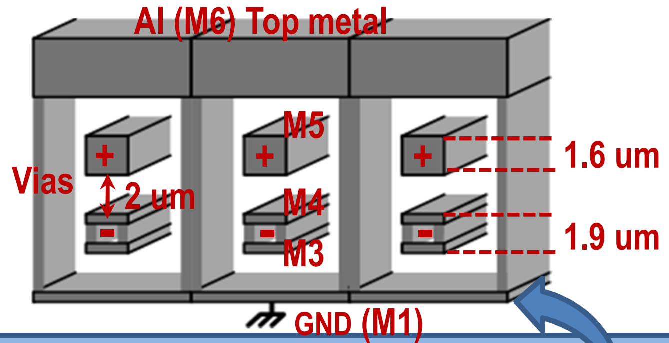


- 0.18-μm SiGe BiCMOS technology
  - 1P6M, f_T=150 GHz
- Size: 2.6 x 3.2 mm^2 (overall)
- Near perfect corporate-feed layout
  - E-length is identical for all channels
- Metallic barrier
  - Grounded via stacks from M1-M6
  - Decrease ch-to-ch coupling
- Current consumption: 724 mA (5 V, 3.6 W)

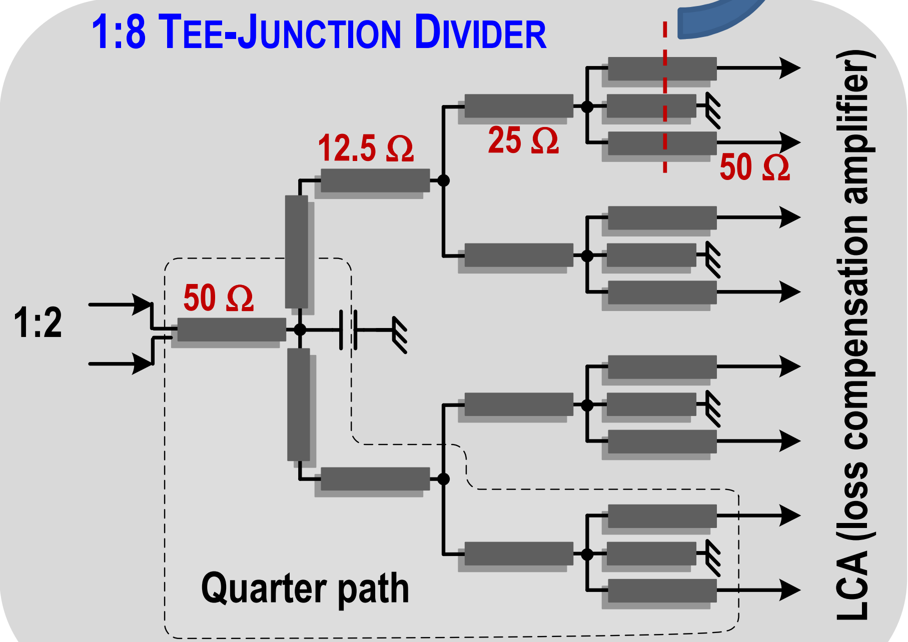


16-element Q-band phased-array Tx (44 GHz, 1:8 T-junction)



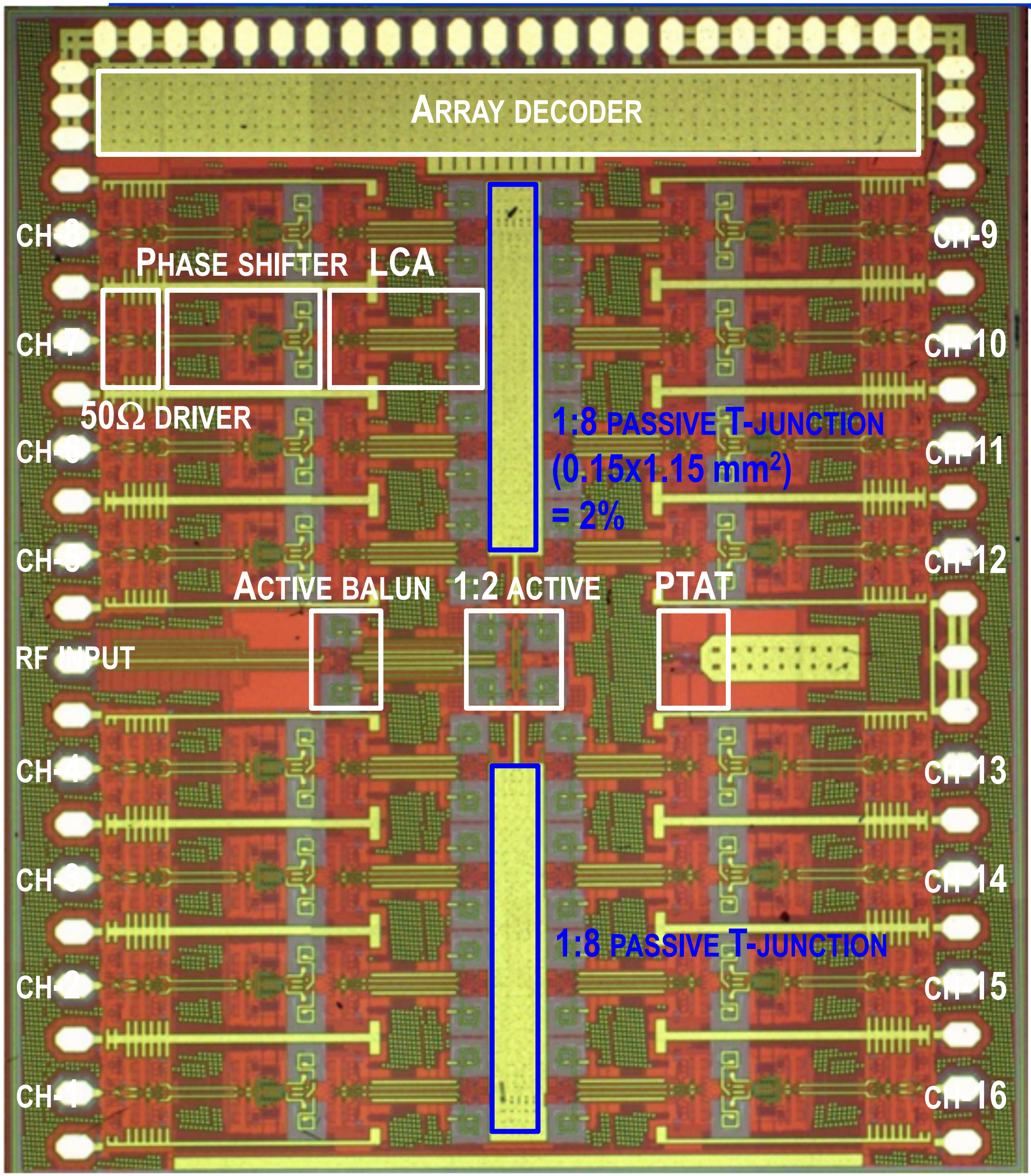


- Perfectly shielded (no coupling btw T-lines)
- Allow compact integration of many diff T-lines

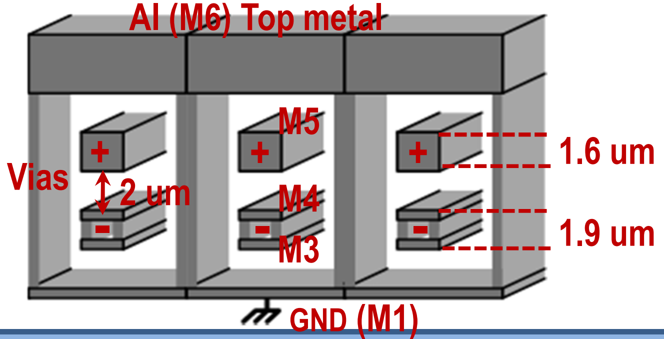


Division loss: 18 dB + parasitic loss (~ 3 dB)

16-element Q-band phased-array Tx (44 GHz, coaxial T-line)

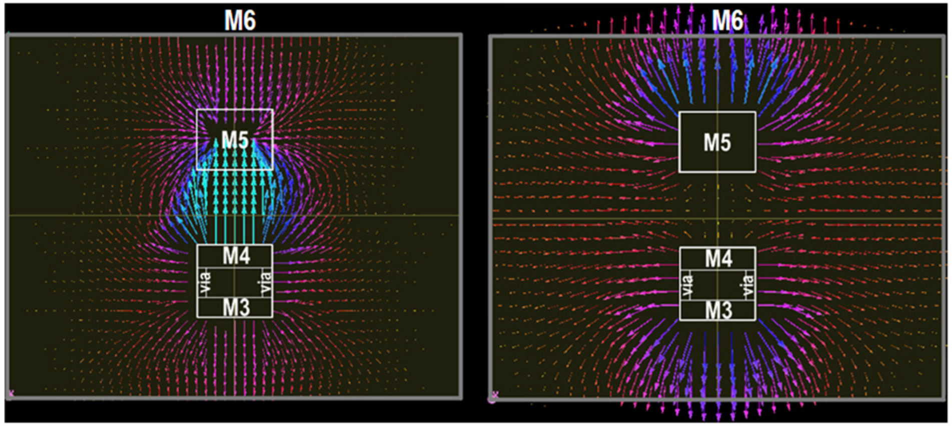


Shielded Broadside-coupled Diff-T-line



- Perfectly shielded (no coupling btw T-lines)
- Allow compact integration of many diff T-lines

Odd-mode E-fields **Even-mode E-fields**



- W=3 μm: odd-mode impedance=50 Ω (HFSS sim)
- Most fields (> 95%) are confined btw diff-T lines
- Measured loss: 3 dB / 0.5 mm @45 GHz

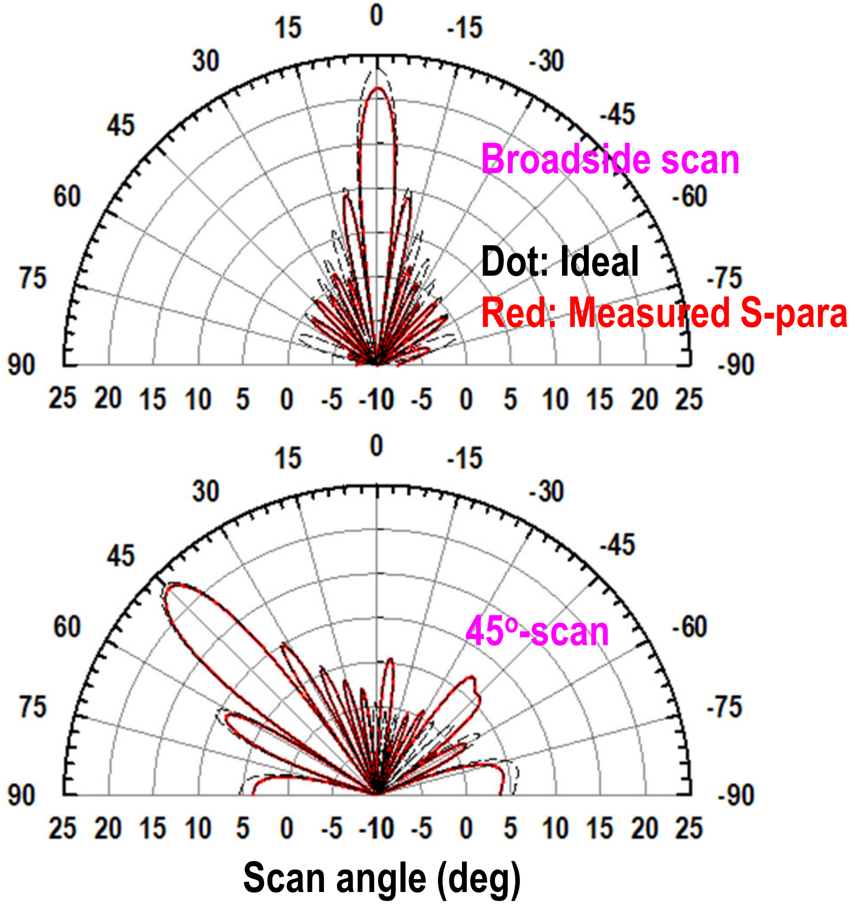
16-element Q-band phased-array Tx (44 GHz, measurement)

Parameter	Results
Technology	0.18-µm SiGe BiCMOS (Jazz SiGe120, 1P6M)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	I_{bias}=720 mA (44 mA per channel)
Frequency band	Q-band (3-dB BW: 40-45.5 GHz)
Phase resolution	4-bit (accuracy > 5-bit)
Input return loss	< -10 dB @ 36.6-50 GHz
Output return loss	< -10 dB @ 37.6-50 GHz
Power gain (ave)	12.5 dB @ 42.5 GHz
Maximum output power	-2.5±1.5 dBm @ 42.5 GHz
Phase error (RMS)	< 8.8° @ 30-50 GHz
Gain error (RMS)	< 1.3 dB @ 30-50 GHz
Output P_{1dB}	-5±1.5 dBm @ 42.5 GHz
Phase mismatch (RMS)	< 7° @ 30-50 GHz (between all channels)
Amp. mismatch (RMS)	< 1.8 dB @ 30-50 GHz (between all channels)
Isolation (CH-to-CH)	< -30 dB @ 30-50 GHz
Array factor directivity	12 dB (16-element)
Chip area	2.6 x3.2 mm²

Single channel

16-array

Beam pattern based on measured S-parameters (16 S-para x 16 channels= 256 S-para)

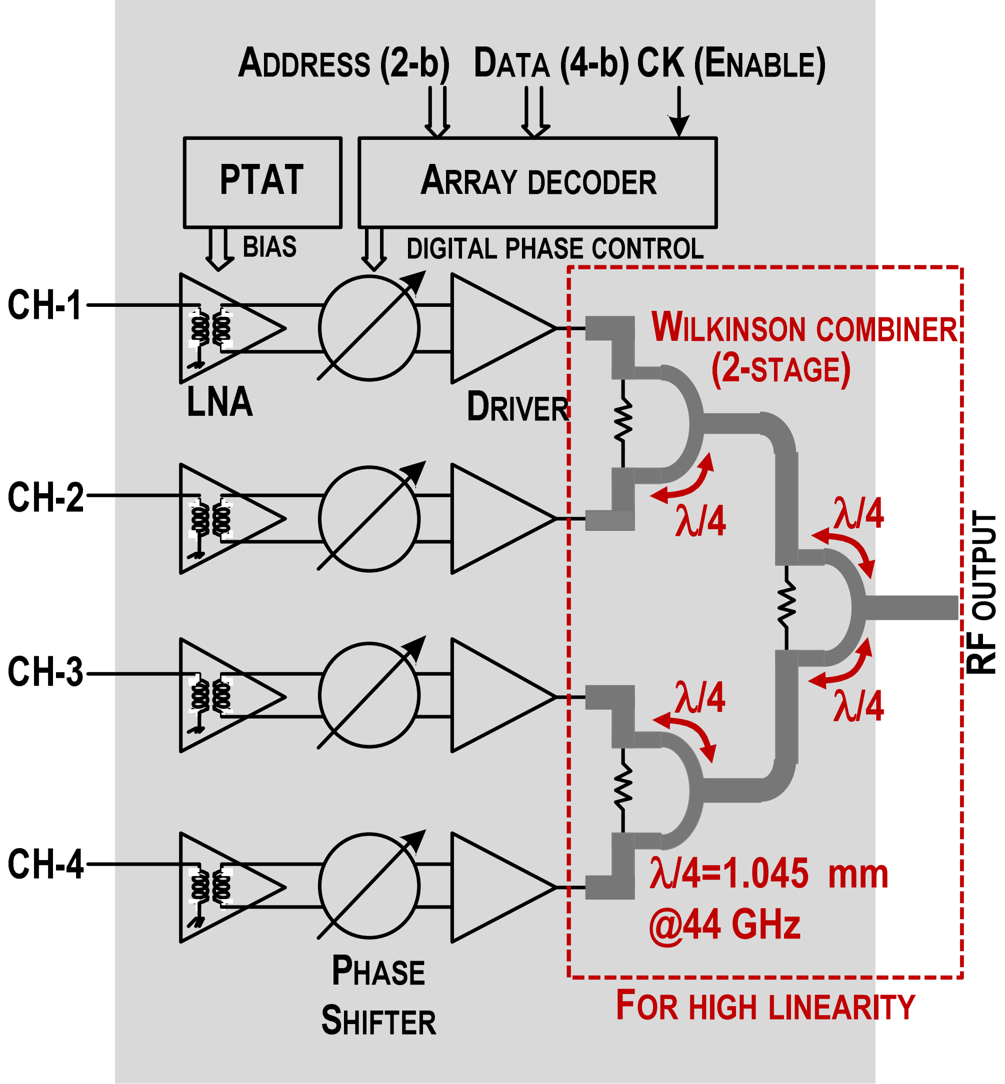


Assumption

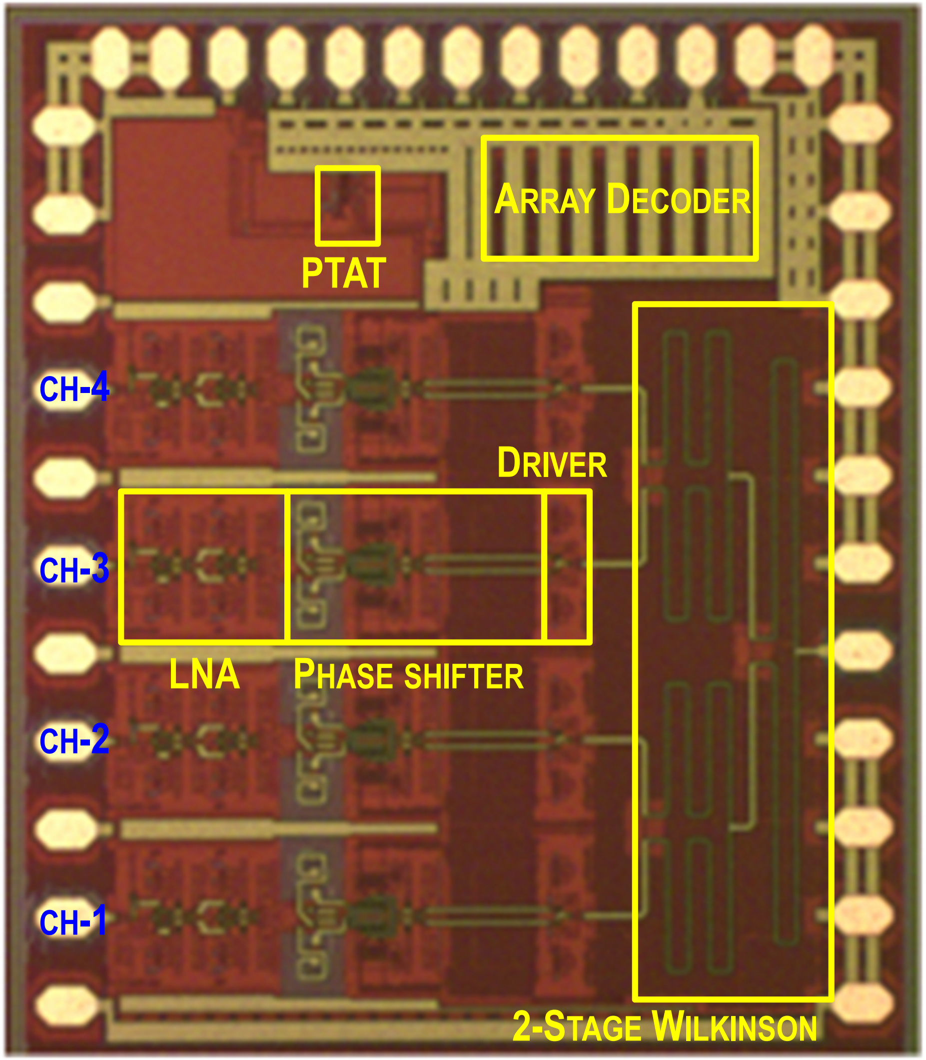
- Isotropic radiator, uniform array spacing, d=λ/2
- Ideal 45°-scan: 127.3° (= 360° x d/λ x sin45°)

4-element Q-band phased-array Rx (44 GHz, arch. & chip photo)

Phased-array Rx block diagram



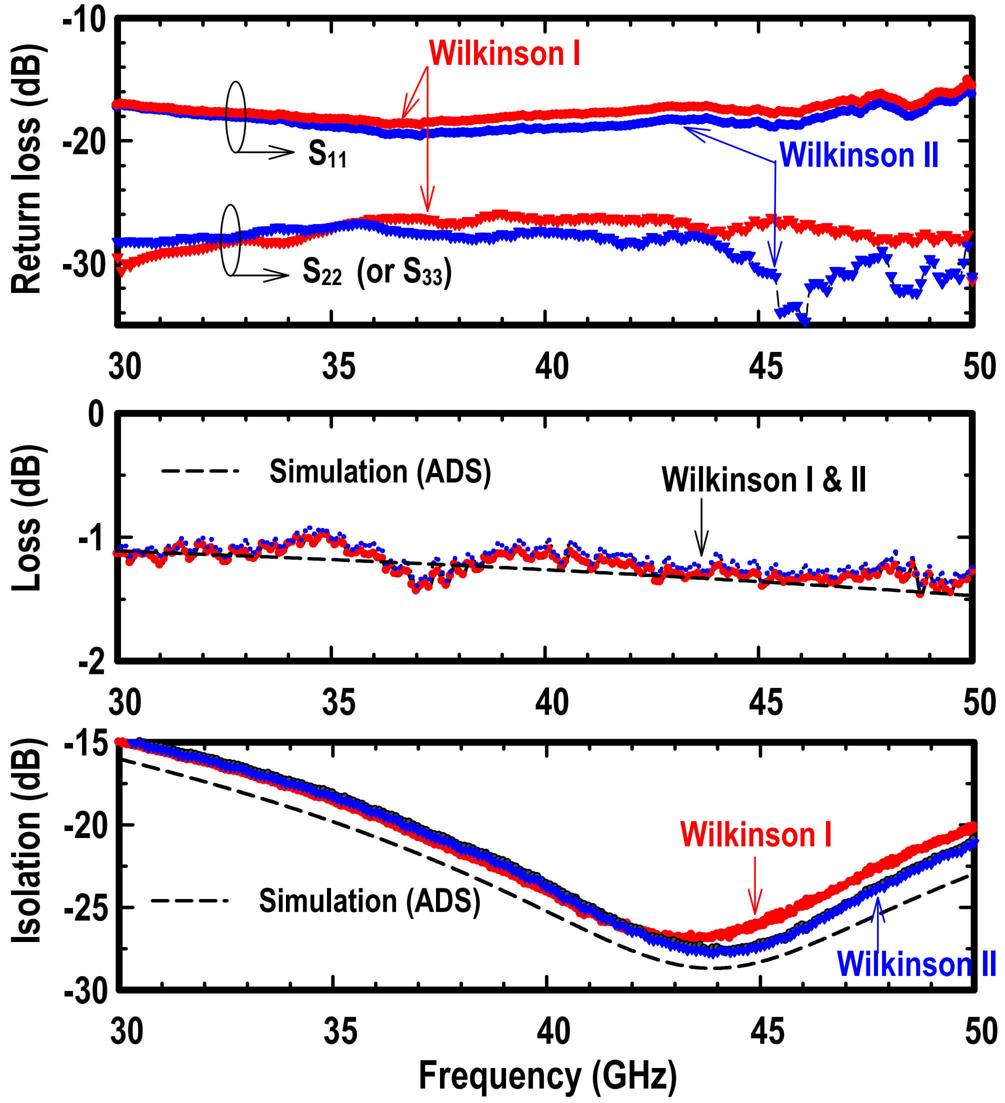
Chip photograph



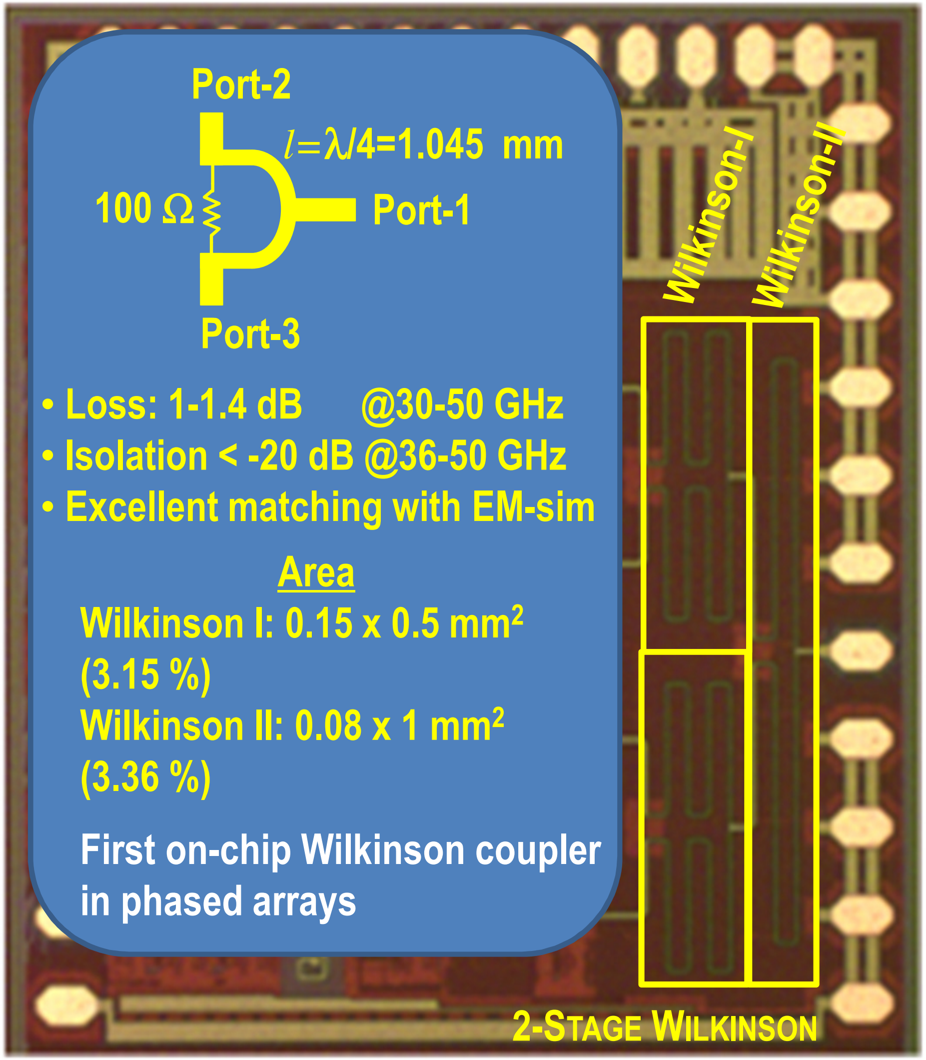
SiGe BiCMOS (f_T=150 GHz), Area=1.4x1.7 mm^2

4-element Q-band phased-array Rx (44 GHz, Wilkinson coupler)

Wilkinson coupler measurements



Chip photograph



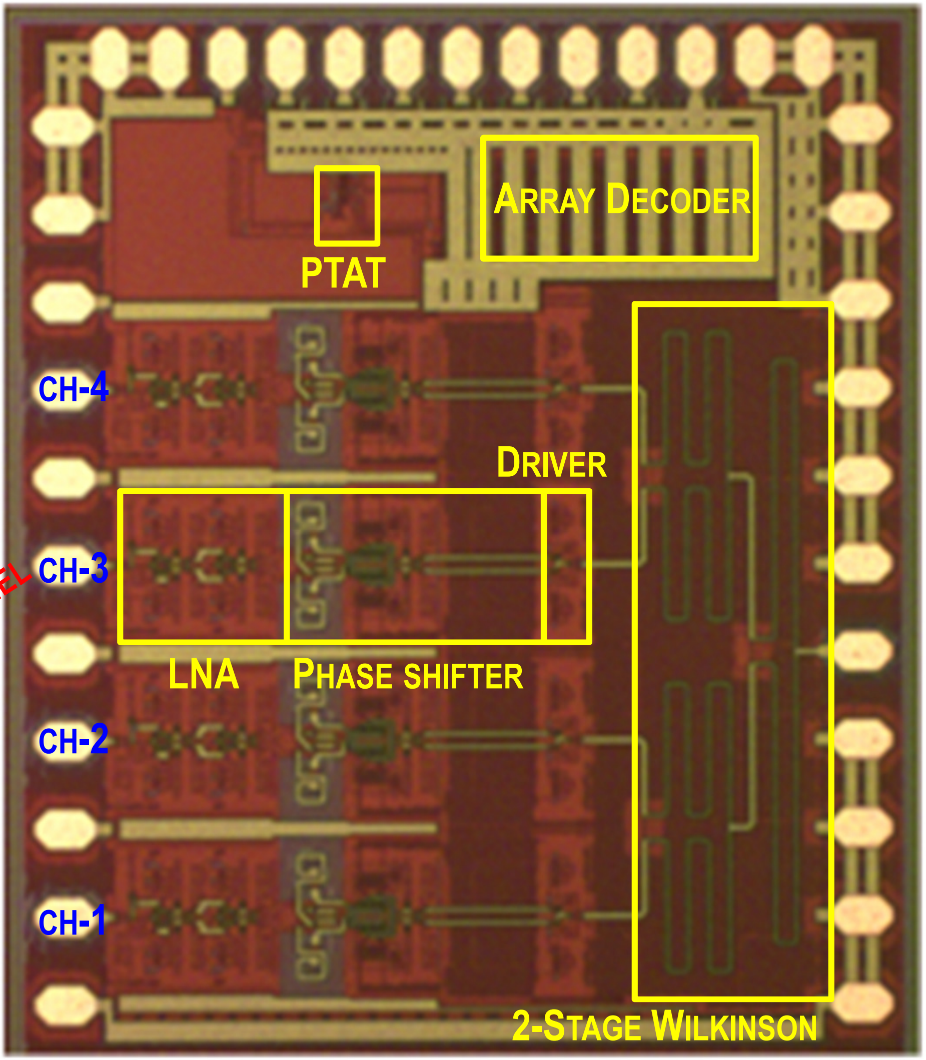
SiGe BiCMOS (f_T=150 GHz), Area=1.4x1.7 mm^2

4-element Q-band phased-array Rx (44 GHz, measurement)

PARAMETER	RESULTS
Technology	0.18-µm SiGe BiCMOS (Jazz SiGe120, 1P6M)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	I_{bias}=118 mA (29 mA per channel)
Frequency band	Q-band (3-dB BW: 32.3-44 GHz)
Phase resolution	4-bit (accuracy > 5-bit)
Input return loss	< -10 dB @ 40-50 GHz
Output return loss	< -10 dB @ 40-50 GHz
Power gain (ave)	10.4 dB @ 38.5 GHz
NF	12.4 dB @ 38.5 GHz
Phase error (RMS)	< 8.7° @ 30-50 GHz
Gain error (RMS)	< 1.2 dB @ 30-50 GHz
IIP3	-13.8±1.5 dBm @ 38.5 GHz
Phase mismatch (RMS)	< 2° @ 30-50 GHz (between all channels)
Amp. mismatch (RMS)	< 0.4 dB @ 30-50 GHz (between all channels)
Isolation (CH-to-CH)	< -35 dB @ 30-50 GHz
Array factor directivity	6 dB (4-element)
Chip area	1.4 x1.7 mm^2

SINGLE CHANNEL

4-ARRAY



Ref: K.-J. Koh *etal,* “A Q-Band Four-Element Phased-Array Front-End Receiver with Integrated Wilkinson Power Combiners in in 0.18-µm SiGe BiCMOS Technology”, IEEE Trans. On MTT, Sept 2008

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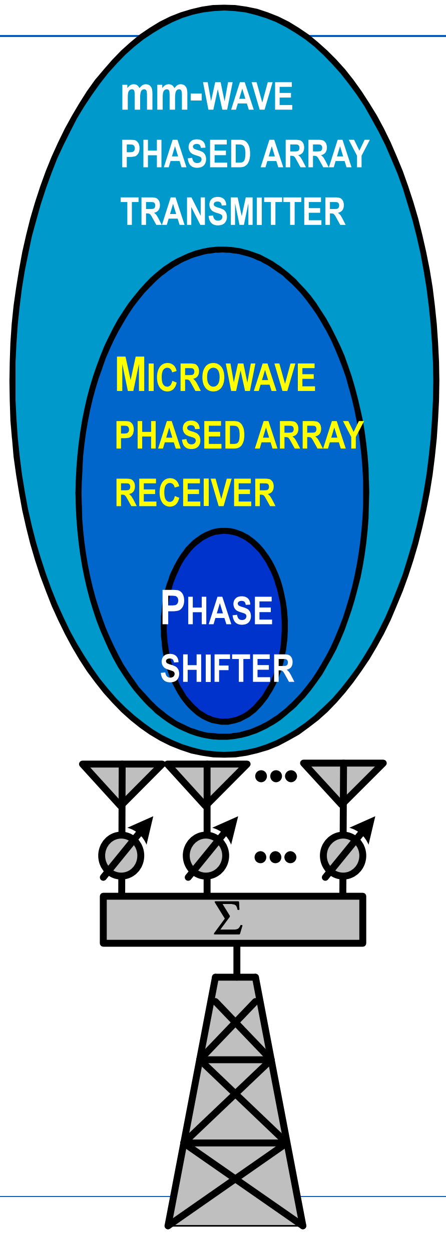
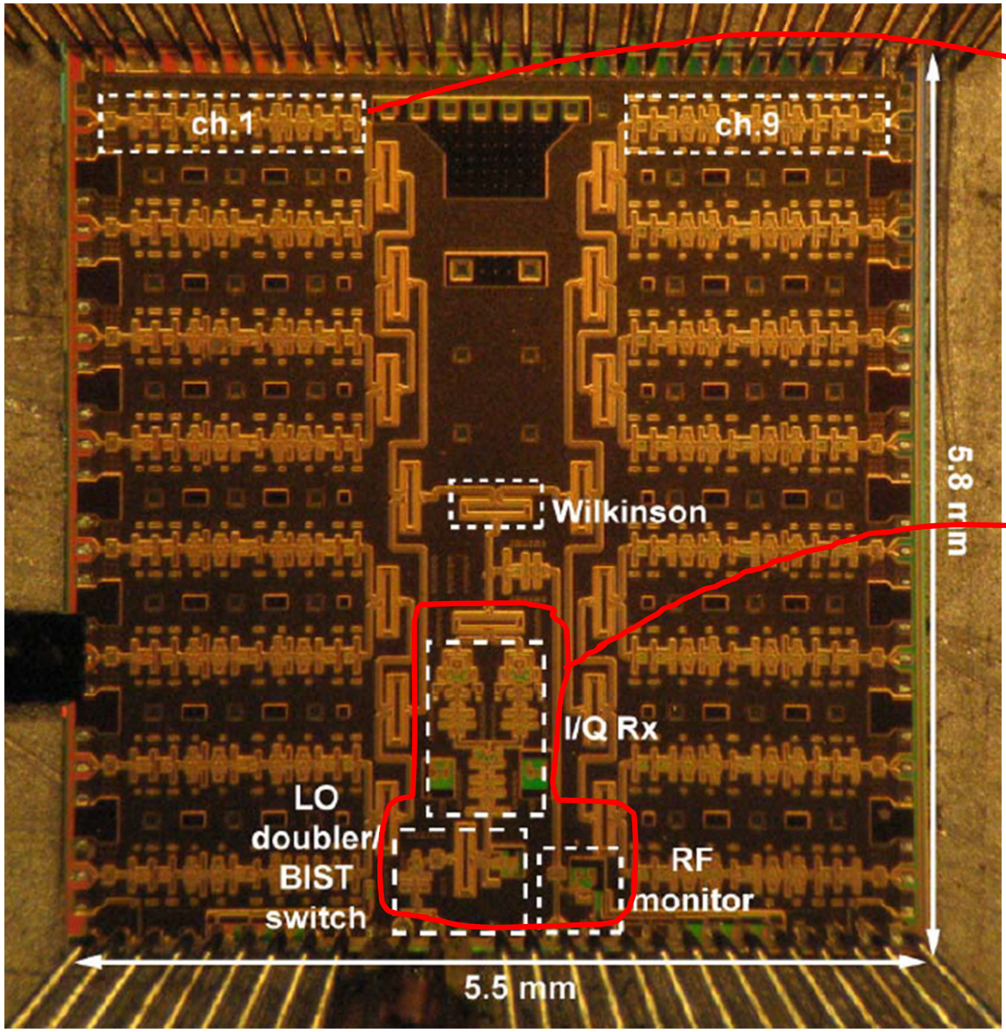
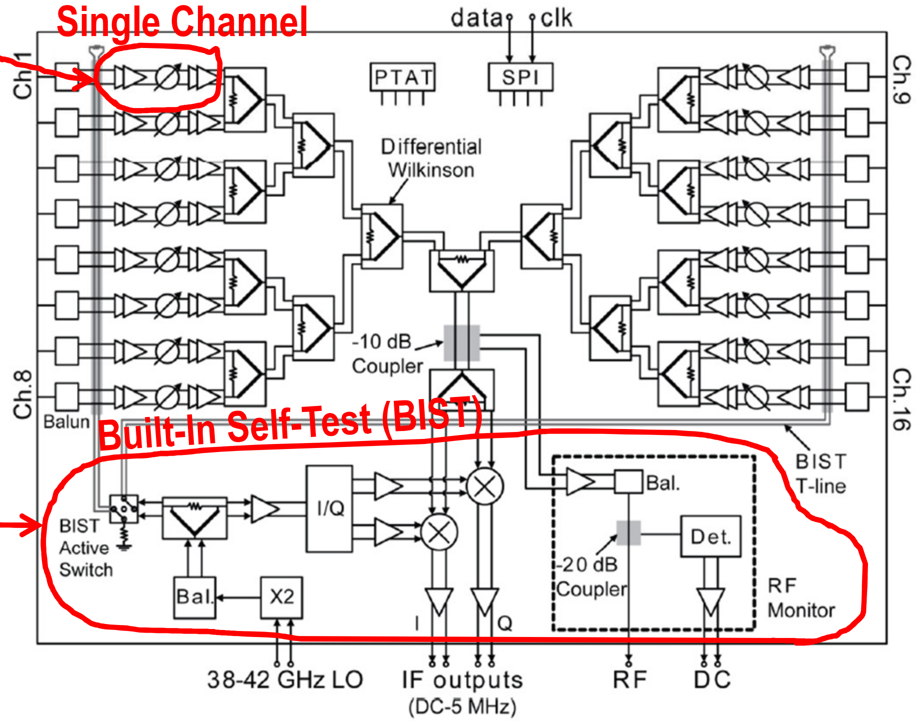


16-element W-band phased-array Rx (77-84 GHz)





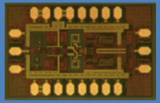
This work is based on passive phase shifter which works fine at W-band due to high-Q & small size inductors (*more results coming soon from UCSD*).

- Automotive radar applications
- All-RF architecture with 4-stage Wilkinsons
- BIST saves time & cost in measurements
- DC power: I_{Bias}=30 mA/channel, V_{DD}=2.1 V
- Gain: 11-16.5 dB @77-83 GHz
- Phase error (rms): < 11° @77-83 GHz
- Gain error (rms): < 0.9 dB @77-83 GHz
- NF: 12 – 13.5 dB @77-83 GHz
- P1dB: -21 dBm @77GHz, -25 dBm @83 GHz

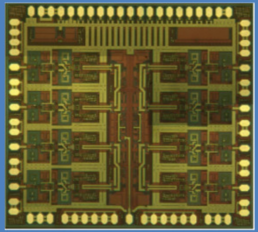
Conclusions

- Provide a low-cost phased array solution for RF and mm-wave defense & commercial applications.
- First implementation of *All-RF (RF-scanning)* Si phased array IC including system-level demonstration.

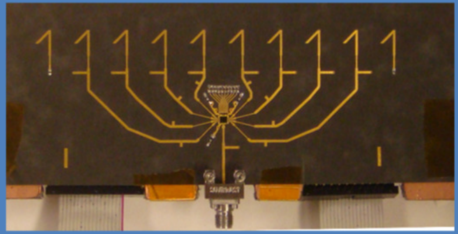
Phase shifter

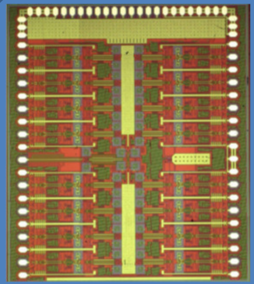


Si on-chip array



Antenna board verification

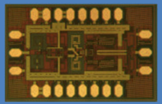




- First 16-element integration in silicon
- First mm-wave (>30 GHz) on-chip silicon array
- Inspire industries (DoD & Commercial)

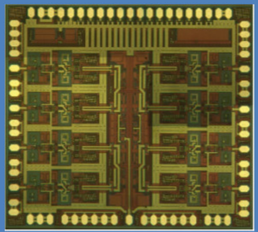
- Successful technology transfers to DoD industries (Boeing, Lockheed Martin, Raytheon, Teledyne, NG).

Phase shifter



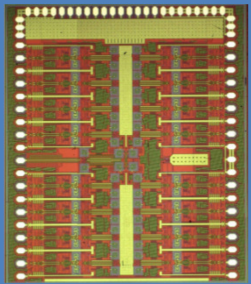
Lockheed Martin (JSSC 2007)

X-band, 8-element Rx



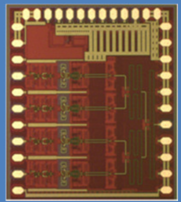
Lockheed Martin Raytheon, Boeing Northrop Grumman (JSSC 2008)

Q-band, 16-element Tx



Teledyne (Rockwell) (JSSC 2009)

Q-band, 4-element Rx



Lockheed Martin Boeing (T-MTT 2008)

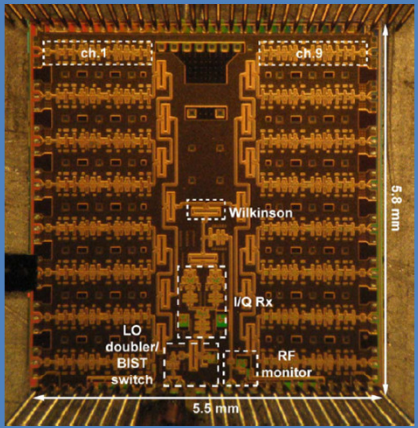
"The Most Significant Achievement in 2007" DARPA Special "WAR REPORT" to Pentagon

"Team of The Year Award in 2010" from Teledyne Scientific Corp (Rockwell)

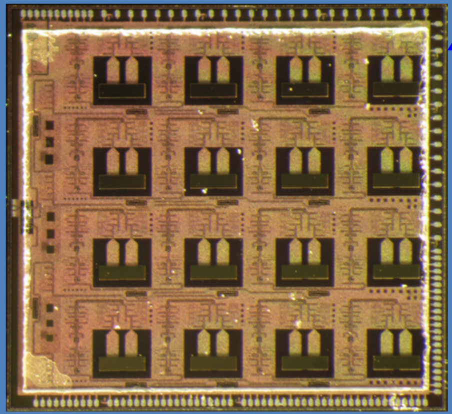
Conclusions

- ❑ ***All-RF Designs*** **can be extended further for W-band and beyond > 100 GHz ranges for radar and high data rate mm-wave comm.**

W-band, 16-element Rx



100-110 GHz, 16-element Tx



This chip integrates 16 Quartz antennas on top of silicon chip (Not presented here, but more results coming from Prof. Rebeiz's group at UCSD) !

Not published yet.

- ❑ **Now, *All-RF* phased-array architecture becomes industry standard in integrated phased array designs (IBM, MTK, Intel … all use the *All-RF* based phased array architecture).**

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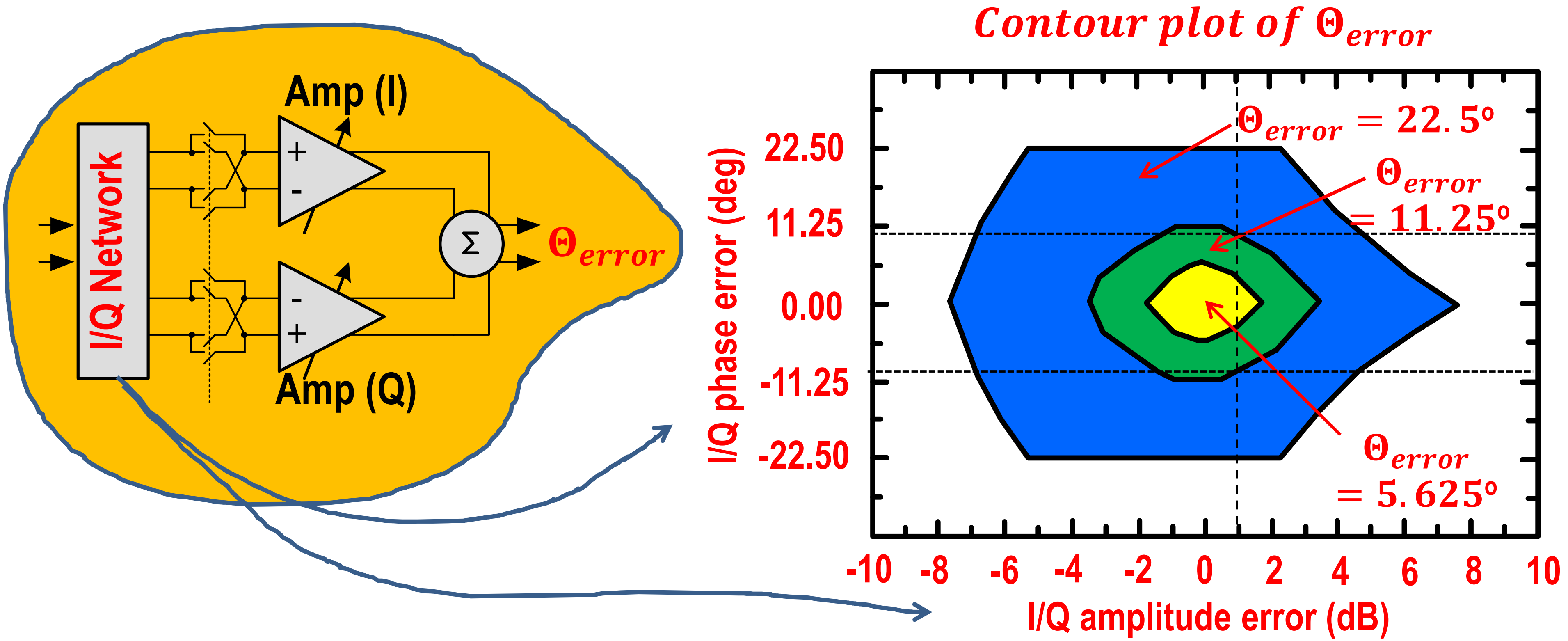
Errors considerations in the active phase shifter (supplementary)



- ❑ Amp (I) and Amp(Q) can be layed out with a good matching.
- ❑ Major error source of output phase will be I/Q network errors (I/Q amp. error, and phase error).
- ❑ Output phase error (Θ_{error}) is a function of combination of I/Q amp. error and phase error.

Ex) For 4-bit accuracy, min phase resolution, $\Delta\theta$= 22.5° → Θ_{error} should be less than $\Delta\theta/2$=11.25°.
Therefore, if I/Q amplitude error is 1dB, then I/Q phase error should be within ~ +/- 10° range.

Details of analysis is presented in Kwang-Jin Koh's Ph.D thesis (2008, UCSD).